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Direct Determination of Quasi-minimal States for Completely-Specified Sequential Circuits

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<Abstract.>

By introducing the characteristic inputs into the concept of internal states, the determination of minimal states has been made more simpler than the methods used so far. Other problems, e.g. hazards, race conditions etc., are not taken into consideration in this paper.

준 최소 상태의 직접결정 방법

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<요 약>

본 논문에서는 특성입력(Characteristic Input)의 개념을 내부변수(Internal State)에 도입함으로서 최소변수를 결정하는 과정이 이제까지의 것 보다 훨씬 간단해졌다. 이 이외의 문제들 예를들어, 장애, 경주 조건 등은 여기에서 취급치 않았으며 몇가지 예에 본 논문에 제시된 방법을 적용한 결과 분할방식이나 관련도표(Implication table)에 의하여 최소변수를 구하는 과정이 아주 간단해짐이 확인되었다.

I. Introduction:

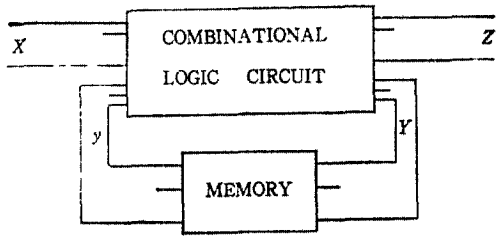

Fig. 1. General Model of Clocked Sequential Circuits.

Geneally the sequential circuits are characterized from the combinational circuits, by thefacts that:

1. They are more economical than the combinational circuits.
2. They are slower in making dicisions or in carrying out a specified objective than the combinational circuits.

Hence, it is, so called, the trade-off problem (speed-versus-cost) which circuit we shall choose for a given logic design.

So far, the synthesis of sequential circuits was realized by the procedures as follows;(1)(2)

(i) Development of a state diagram.
(ii) Setting up a state table from step (i).
(iii) Getting the minimal state table by eliminating the redundant states.
(iv) State assignment.
(v) Completing the Y-map and Z-map.

(vi) Finding out a suitable set of Boolean expressions.

(vii) Circuit Realization.

The general model of sequential circuits is shown in Fig. 1. The y's denotes the secondaies; Y's excitations; X's, the input; Z, output.

Ⅱ. Brief Discussion of the Current Method

To realize the logic circuit from word statements, we must first draw a state diagram, make a state transition table from this diagram, and then eliminate the redundant states as introduecd in section Ⅰ.

To obtain a state diagram, we must consider all the possible inputs which determine the intenal states.

Therefore, it is inevitable that this diagram comprises many states.

Untill now the partitioning method (2) and Implicaion table (2) have been the most powerful tools for obtaining the minimal states.

However, with a lot of states, the above-mentioned two methods become very complex and time-consuming. So there arises a need to reduce the mumber of states from the beginning. There were strong evidenes (4) that final minimal state table had some relation with the properties of input, and this is the basis of the approach considered in this paper.

Ⅲ. Determination of states.

To clarify the concept imposed and to simplify the procedure, we shall confine ourselves to single-input single-output systems. But this method to be treated here can easily be extended to multi-input multi-output systems. The input variables are a sequence of x_i's where x_i can take only "0" or "1".

Suppose we want to have an output "1" for a sepecified sequence of inputs, namely

$X=(x_1, x_2, \ldots, x_n)$ $x_i \varepsilon \{0,1\}$ $i=1,2,\ldots,n$ (1)

※ See reference book (1) page 193—194 and reference (2) chap. 10

Definition:

A CHARACTERISTIC INPUT is a sequence of inputs followng the successful one or ones from the first.

For example, (x_1) singly is the first characteristic input, (x_1x_2) the second characteristic input and $(x_1x_2,\ldots x_n)$ is the final characteristic input. So there are n characteristic inputs for the problem c nsidered here.

Definition:

"Q-state (q_0)" is a set of states which received inputs other than the characteristic inputs.

To be more specific, we define the states associated with the characteristic inputs as follows:

q_1: the state which receives the first successful input from the Q-state.

q_2: the state which receives the second successful one from the q_1 state, that is, associated with the second characteristic input.

q_i $(i=3,\ldots n)$ are defined in a similar fashion.

Now we are in the position to determine the internal states for any sequential inputs. With the $(n+1)$ states defined above, we can determine all the states for any input. Hence the following theorem is evident.

Theorem: In the clocked sequential circuit, there are at most $(m+1)$ states for the given input sequence $(x_1x_2, \ldots x_m)$ which produces an output 1 at the instant final input x_m has arrived.

Proof: From the definition of q_i $(i=1,\ldots m)$, it is seen that any input sequence either falls in q_i or belongs to q_0. Therefore we have $(m+1)$ states at most. Q.E.D.

Whether these $(m+1)$ states are the minimal states or not is a question to be studied. But at any rate the states are limited to $(m+1)$ states, Which are more feasible to treat than the ones by current method.

Ⅳ. Synthesis of Sequential Circuits.

The design of sequential circuits for an example will be considered to show how easily the

state table can be obtained.

—Example—

We consider a sequential machine which emits a "1" at the time immediately after the arrival of the last input if it receives "0010".

Solution: The characteristic inputs for q_1, q_2, q_3, q_4 are "O", "00", "001", and "0010", respectively.

The state diagram is drawn like fig. 2 comparing the inputs with the characteristic inputs.

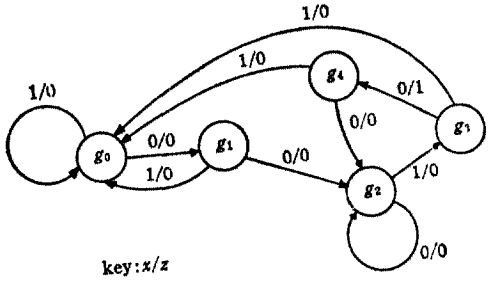

Fig. 2 Development of state diagram.

Table 1 shows the stats table obtained. If the computer is available, this table can be obtained indi rectly by computer.

	Y		Z	
	$X=0$	$X=1$	$X=0$	$X=1$
q_0	q_1	q_0	0	0
q_1	q_2	q_0	0	0
q_2	q_2	q_3	0	0
q_3	q_4	q_0	1	0
q_4	q_2	q_0	0	0

Table 1 State table.

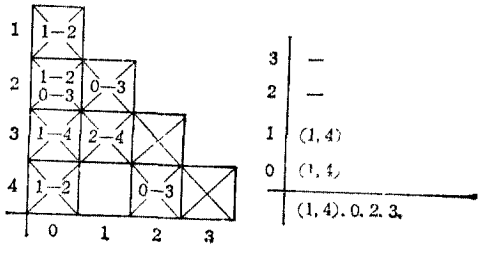

Table 2. Implication table

We now check the redundant states by completing an implicition table as in table 2.

From table 2 the minimal state is acquired as in fig 3.

	Y		Z	
	$x=0$	$x=1$	$x=0$	$x=1$
q_0	q_1	q_0	0	0
q_1	q_2	q_0	0	0
q_2	q_2	q_3	0	0
q_3	q_1	q_0	1	0

Fig. 3 Minimal State Table

As the above example reveals, the minimal state table is more easily acquired than the conventional method. The final circuit realization using S-C flip-flops is presented here(Fig 6) along with Y-map (Fig. 4), Z-map, Excitation map (Fig. 5) and a set of Boolean equations. The detailed procedures can be found in the texts (1)(2)(3)

y^ν	$y_2\ y_1$	$x=0$	$x=1$	$x=0$	$x=1$
q^ν	0 0	0	0	1	0
q_1	0 1	1	0	1	0
q_2	1 1	1	1	1	0
q_3	1 0	0	0	1	0
		$Y_2=y_2^{\nu+1}$		$Y_1=y_1^{\nu+1}$	

Fig. 4 Next state map.

	x		x		x		x		x	
$y_2\ y_1$	0	1	0	1	0	1	0	1	0	1
0 0	0	0	×	×	1	0	0	×	0	0
0 1	1	0	0	×	×	0	0	1	0	0
1 1	×	×	0	0	×	0	0	1	0	0
1 0	0	0	1	1	1	0	0	1	1	0
	Sy_2		Cy_2		Sy_1		Cy_1		z	

x denotes don't-care terms

Fig. 5 Excitation maps.

The final set of Boolean equations are

$$S_{y2}=y_1\bar{x}\quad S_{y1}=\bar{x}\quad C_{y2}=\bar{y}_1y_2\quad C_{y1}=x\quad Z=\bar{x}\bar{y}_1y_2$$

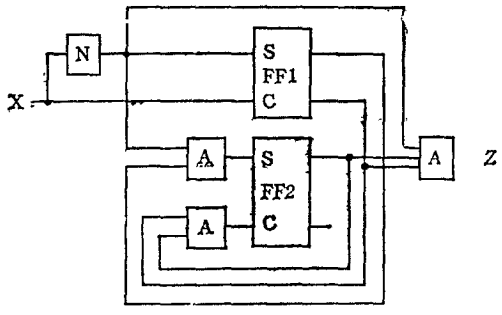

Fig. 6. Circuit Realization of the Problem

V. Conclusion

We see that the design procedure concerning the minimal state table may be made very simple by the concepts of characteristic input and Q-state.

It is the author's opinion that this method can be computerized with ease if some revisions are added.

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