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A Very Efficient R-F Power Amplifier Circuit

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〈Abstract〉

The efficiency of the device and the circuitry is very important in an r-f power generation circuit. In this paper a study is made to see if any intrinsic operating characteristics of transistors, unipolar types in particular, can advantageously be utilized to generate r-f power effectively.

A conventional class C FET r-f power amplifier is analyzed following a semigraphical method similar to that used for vacuum tubes. Some advantageous characteristics of the device are discussed.

The applicability of FETs to pulse-excited r-f power generation circuit is investigated and the device limitations in this field of application are discussed.

Finally, the combined use of an FET and a conventional bipolar transistor, to overcome the respective limitations, in an efficient r-f power generation circuit is studied. A practical working model of this hybrid circuit whose conversion efficiency is much higher than those of conventional class C r-f power amplifier was built and tested to illustrate its advantages.

전환 효율이 높은 무선주파 전력 증폭기회로

박 원 심
전기공학과

〈요 약〉

무선주파 전력 증폭기 회로에서는 그 회로와 거기에 사용된 회로소자의 효율문제가 중요시 된다. 본 논문에서는 Transistor, 특히 단일 극성형인 FEF의 고유동작 특성을 유효하게 이용함으로써 무선주파 전력 증폭회로의 전환효율을 증대시키는 방안을 모색하였다.

먼저 C급 FET 무선주파 전력증폭기회로를 종전의 진공관 회로분석에 사용되는 반도해석 방법에 따라 분석하고 몇가지 유리한 특성들을 들었다.

다음으로 Pulse 여진형 FET 무선주파 전력 증폭기회로를 분석하고 이 회로소자의 특성상 한계를 논하였다.

끝으로 쌍극성 Transistor와 단일극성형인 Transistor의 단점을 각각 보완하도록 혼성회로를 구성하고 그 회로모델을 조립 시험한 다음 그 결과를 제시하여 이 혼성회로의 전환효율이 종래의 C급 전력 증폭기보다 훨씬 높음을 실제로 보였다.

I. Introduction

There are many applications in which amplitude linearity between input and output is not necessary but efficiency of the device and the circuitry is very important. An immediate example of this type of applications is an emergency

life-boat transmitter where input power is limited and expensive to provide. In connection with this type of applications, transistors - both bipolar and unipolar types - possess several superior characteristics over the vacuum tubes. The purpose of this study is to see if any of these intrinsic operating characteristics can advantageously be used for improving the conversion efficiency of an r-f power amplifier circuit. In this paper, unipolar transistor applications are investigated exclusively since there are many application notes on bipolar transitors available in the literature.

The result of this study evolves a type of radio-frequency amplifier circuit whose efficiency with regard to r-f power output for a given d-c input power is much higher than those of conventional class C amplifier. The reasons for this high efficiency are the combined operating effects of extremely high input impedance Metal-Oxide-Semiconductor Field-Effect Transistor and a bipolar transistor operating in a pure switching mode.

To arrive at this result, a MOSFET conventional class C r-f power amplifier circuit was examined and then a pulse excited r-f power amplifier circuit was studied with particular attention paid to the advantageous utilization of device characteristics in improving overall system efficiency. Finding that the saturation resistances of unipolar transistors the author could find were higher than those of standard bipolar switching transistors available, a hybrid application was attempted. This hybrid circuit presents a very high conversion efficiency. To illustrate this, a model of the circuit was built and tested in the laboratory.

Ⅱ. Class C R-F Power Amplifier

High efficiency is extremely important in the r-f power generation stage, not only in economizing on the supplied power but also in permitting large power output to be obtained from relatively small devices; both of which the transistor user often desires. These prime objectives of r-f power amplifiers are achieved by operating the device in the claass C mode of operation.

As for conventional vacuum tube class C r-f amplifiers, class C operation occurs when the drain current conduction angle is less than 180 degrees. High efficiency in class C operation is the result of the fact that the drain source supply voltage V_{DD} supplies energy to the amplifier only when the largest portion of this energy will be absorbed by the tuned circuit at the drain, maintaining a low power dissipation in the device. This relationship can be seen from the oscillograms of class C r-f amplifier drain voltage, gate voltage and drain current wave forms

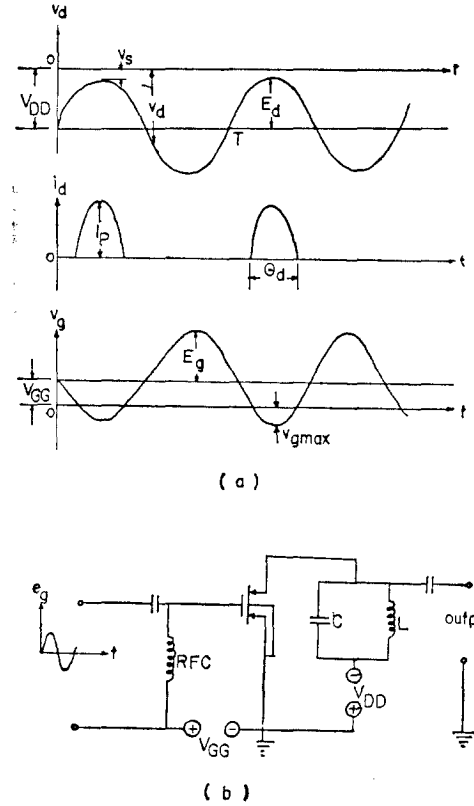


Fig. 1 a. Class C r-f Amplifier Drain, Gate Voltages and Drain Current Wave Forms (P-channel device)

b. Basic Class C FET Amplifier Circuit Configuration

illustrated in figure 1a. The basic class C amplifier circuit with a parallel tuned load is shown in figure 1b.

Considering the limitations of some FET types, the following discussion of FET application to the conventional class C r-f power amplifier configuration is directed only to the insulated gate type field-effect transistor. In particular, an enhancement mode MOSFET is used as an example. As with the vacuum tube counterpart, a mathematical analysis of the class C tuned FET amplifier is complicated and the use of design charts is a plausible approach. Although this method is only approximate and lengthy, it is directly useful in design since an explicit solution for the optimum operating conditions can be obtained from the semigraphical analysis (1).

To get specific results from the investigation, an r-f power amplifier stage is analyzed for several operating conditions using an FN 1034 p-channel enhancement mode MOSFET. The illustration shows that the efficiency or the power output can be maximized by proper choice of the device and the operating conditions. Several advantages of FETs revealed by above illustration were as follows:

From the extremely high input impedance characteristics of the MOSFET, the excitation power required is very small and the driver stage can be a simple voltage output device with very small power. By proper choice of the device, class C operation can be achieved without biasing, thus enhancing the overall circuit efficiency. Proper combination of V_{DD} and E_g reduces Millar Effect for high frequency application, since voltage gain under this condition is approximately unity.

3. Pulse-Excited R-F Power Amplifier Circuit

A pulse-excited switching-mode r-f power amplifier circuit is another form of circuit configuration which gives high effieieucy. In the following study, the operating performance and the design considerations of the pulse-excited r-f amplifier stage are discussed. At the end of section, a design example is given using a Crystalonics' power field-effect transistor CP603.

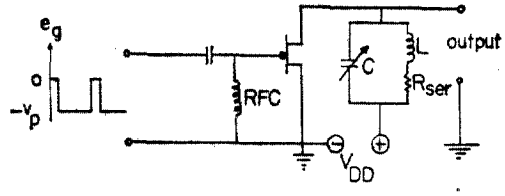


Fig. 2. Basic Tuned Amplifier Circuit (N-channel FET)

A Typical parallel tuned circuit configuration is shown in figure 2. The circuit connencted in the drain circuit of the device is very seldom, if ever, a simple parallel arrangement such as shown in figure 2. For proper operation of the device the required impedance at the device output terminals is fixed, and the actual load impedance is generally also fixed by external load conditions. Although a more complicated circuit is connected to the device output terminals to perform necessary impedance transformations mentioned above, the coupling network and load can usually be reduced to an equivalent simple parallel tuned circuit at a particular frequency. In figure 2, R_{ser} includes the coupled resistance from the actual load.

The loaded Q, Q_L of the drain tank circuit, $\omega_0 L/R_{ser}$, should be high to provide reasonable discrimination against the harmonic components contained in the drain current pulses. In practice, Q_L of 10 represents a typical value (2). At the same time, the input impedance of the drain tank circuit must meet the device operating condition,

$$R_t = \frac{E_{dl}}{I_{dl}} \qquad (3-1)$$

Where R_t is the impedance at resonance, E_{dl} and I_{dl} are the amplitudes of the fundamental components of the drain voltage and current. E_{dl} and I_{dl} will be determined in the subsequent development. This value of input impedance is related to the drain tank circuit components

values and Q_L by the relatin (1),

$$R_l=Q_L\sqrt{\frac{L}{C}}=\frac{L}{R_{ser}C}=\frac{(\omega_o L)^2}{R_{ser}} \qquad (3-2)$$

From these relations, the value of the input im pedance required by the device can be obtained by simultaneous selection of Q_L and the L/C ratio of the tank circuit.

For the determination of E_{dl} and I_{dl}, and the evaluation of the performance of the circuit, the gate input voltage, drain current and drain voltage wave forms shown in figure 3 will be used.

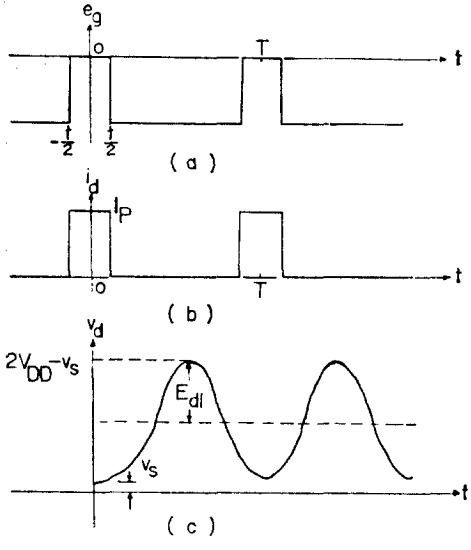


Fig. 3. Gate Voltage(a), Drain Current(b) and Drain Voltage(c) Wave Forms

The value of I_p is obtained from the manufacturer's specification sheets. The average value of the drain current, I, is given by;

$$\begin{aligned} I&=\frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} i_d\,dt \\ &=\frac{1}{T}\int_{-\frac{t_o}{2}}^{\frac{t_o}{2}} I_p\,dt \\ &=\frac{I_p}{T}t_o \end{aligned} \qquad (3-3)$$

where T is the period of input pulse and t_o is the conduction time. The amplitude of the fundamental component of the drain current, I_{dl}, is obtained from the relation;

$$\begin{aligned} I_{dl}&=\frac{2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} i_d\cos\frac{2\pi}{T}t\,dt \\ &=\frac{2}{T}\int_{-\frac{t_o}{2}}^{\frac{t_o}{2}} I_p\cos\frac{2\pi}{T}t\,dt \\ &=\frac{2I_p}{\pi}\sin\frac{\pi}{T}t_o \end{aligned} \qquad (3-4)$$

The amplitude of the fundamental component of alternating drain voltage E_{dl} is;

$$E_{dl}=|V_{DD}|-V_s \qquad (3-5)$$

where V_s is the saturation voltage across the device during maximum current conduction and is dependent upon the value of saturion restance of the device at a particular I_p. Substituting equations (3—4) and (3—5) into equation (3—1), the load impedance required for the device operating conditions is obtained in terms of known quantities.

$$\begin{aligned} R_l&=\frac{E_{dl}}{I_{dl}} \\ &=\frac{V_{DD}-V_s}{\frac{2I_p}{\pi}\sin\frac{\pi}{T}t_o} \quad \text{or} \\ &=\frac{\pi(V_{DD}-V_s)}{2I_p\sin\frac{\pi}{T}t_o} \end{aligned} \qquad (3-6)$$

To evaluate the performance of the circuit, the drain efficiency is examined. By definition the drain efficiency is given by;

$$\text{drain efficiency}=\frac{P_L}{P_{in}}$$

where P_{in} is the dc power supplied to the drain circuit and P_L is the ac power output.

$$P_{in}=V_{DD}I$$

Substituting equaton (3—3) into the above relation;

$$P_{in}=\frac{t_o}{T}V_{DD}\,I_p \qquad (3-7)$$

Output power is given by:

$$P_L=P_{in}-P_d$$

Where P_d is the power dissipated in the device and is computed by the relation:

$$P_d=\frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} V_d\, i_d\, dt$$

$$=\frac{1}{T}\int_{-\frac{t_o}{2}}^{\frac{t_o}{2}} I_p\left(V_{DD}-(V_{DD}-V_S)\cos\frac{2\pi}{T}t\right)dt$$

$$=\frac{I_p}{T}\left(V_{DD}t_o-\frac{T}{\pi}(V_{DD}-V_S)\sin\frac{\pi}{T}t_o\right) \quad (3-8)$$

$$P_L=\frac{I_p}{\pi}(V_{DD}-V_S)\sin\frac{\pi}{T}t_o \quad (3-9)$$

Therefore the drain efficiency is:

$$\text{drain eff.}=\frac{\frac{I_p}{\pi}(V_{DD}-V_S)\sin\frac{\pi}{T}t_o}{V_{DD}\,I_p\frac{t_o}{T}}$$

$$=\frac{T(V_{DD}-V_S)}{\pi V_{DD}t_o}\sin\frac{\pi}{T}t_o \quad (3-10)$$

From equation (3—10) , it is seen that the smaller the value t_o the higher the drain efficiency. Also the drain efficiency is dependent upon the saturation voltage across the device. Hence, a device having small V_S is desirable for this type of operation. To illustrate the foregoing discussion a circuit example will be given along with design procedures.

Assume that an r-f power source of about 200 milliwatts output to a 220 ohm load at an operating frequency of 500 khz is to be designed using an FET. As mentioned at the beginning of this section, the load to which the specified ac power is to be delivered is thus fixed. Since the drain tank circnit impedance required for the proper operation of the circuit is also fixed by equation (3—6), the drain tank circuit including the specified load must satisfy relation (3—6) and at the same time optimum power must be delivered to the actual load with minimum dissipation in the intermediate connecting circuitry. For a first approximation, assume that the coupling circuit efficiency can be made very high. This assumption is reasonable since our load is reasonably large compared to the loss resistances associated with the L and C coupling network. From equation (3—9)

$$P_L=(V_{DD}-V_S)\sin\frac{\pi}{T}t_o$$

Choosing a conduction angle of $\pi/2$ or $t_o=T/4$,

$$P_L=(V_{DD}-V_S)\frac{1}{\sqrt{2}} \text{ or}$$

$$\sqrt{2}\pi P_L-I_P(V_{DD}-V_S) \quad (3-11)$$

Any device which can satisfy equation (3—11) will meet the requirements. In this example, however, the FET in hand (Crystalonics' CP603 Junction power FET) is used. The I_p given in the specification sheet is 180 milliamperes at $V_{GS}=0$, $V_{DS}=5$ volts$=V_S$. Without further calculation, we can immediately see that this device will give poor efficiency because of its comparatively large saturation voltage. Again referring to the absolute maximum rating in the specification sheet, $V_{DD}=10$ volts will give the required output power. A drain efficiency of about 50% can be expected, which is very poor. If, instead of a CP603, we could find a device with a lower value of V_S, for instance, $V_S=0.1$ volts, the drain efficiency would be about 89% as determined from equation (3—10).

The load impedance required for the device operating conditions at the desired resonant frequency is obtained from equation 3—6).

$$R_t=\frac{\pi(V_{DD}-V_S)}{2I_p\sin\frac{\pi}{T}t_o}$$

$$=\frac{3.14\times15}{2\times180\times10^{-3}\times1.414}$$

$$\cong 33 \text{ ohm}$$

Since this required tank circuit impedance at the operating frequency is very low compared to the external load, an ordinary parallel tank circuit with impedance transforming, used in the conventional high outpnt impedance circuits, cannot be used. However, as can be seen from the relation (3—6), R_t depends on $(V_{DD}-V_S)$ and I_p with t_o fixed. When this relation gives a very high R_t compared to the external load, an ordinary parallel tank circuit can be used. In this illustrative example R_t is less than the

actual load and therefore another impedance transforming circuit shown in figure 4 will be used.

C_1 = .02 μf C_2 = .0965 μf C_3 = .0376 μf
R_1 = 22 M R_L = 220 ohm L = 3.74 μh
RFC = 3 mh, .7 ohm V_{DD} = 10 volts

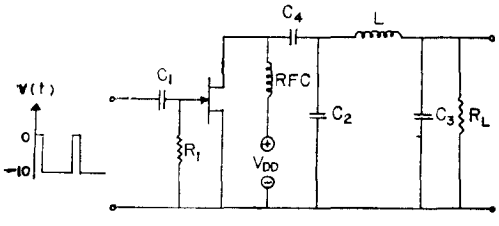


Fig. 4 Circuit for Design Example

This π-coupling network is adjusted to transform, at the operating resonant frequency, the 220 ohm load to 33 ohm as required to match the impedance of the device. This particular coupling network has the advantage of better harmonic suppression characteristics due to the shunt-capacitive arms. The design procedures for this impedance transforming network are found in many standard text books.

Choosing the value of Q_L =10, for reasonable harmonic suppression and relatively low losses in the L-C circuit, the π-network component values at the operating frequency are computed acording to the procedures given in the reference (3).

The efficiency of this amplifier is limited primarily by the large saturation resistance of the FET which the author could find one for illustive calculation. Since there are many bipolar transistors which have much lower saturation resistance, consideration is now given, in the following section, to the combined use of bipolar and unipolar transistors in an efficient r-f power amplifier circuit.

Ⅳ. A Very Efficient Hybrid Circuit

If FETs and bipolar transistors are used in combination, certain superior characteristics of one type to the other may be selectively employed in a circuit operation. One application of this nature is investigated in this section. With the bipolar transistor alone, one of the r-f power generation circuit design objectives of low excitation power requirement is missing due to the inherent low input impedance charactistics of bipolar transtors, unless some other compensating scheme is employed.

For the compensation of this disadvantage, a high input impedance field-effect transistor can be used in the input circuit of conventional device r-f power generator in such a way that the input impedance of the whole stage is high. To justify and illustrate the above statements, an actual working circuit model is given below with laboratory test results.

The final amplifier stage used here is the series-tuned switching-mode transistor r-f power amplifier circuit developed by Dr. Ewing in reference 4. This circuit is chosen since it gives the highest possible efficiency among many other existing circuits. The extremely high collector efficiency provided by this circuit configuration may be combined with a very high input impedance FET excitation stage which requires very low excitation power thereby increasing the power gain and the overall efficiency. The illustrative circuit model with its component values is shown in figure 5. These component values are obtained from calculations using the design formulas and detailed adjustment procedures

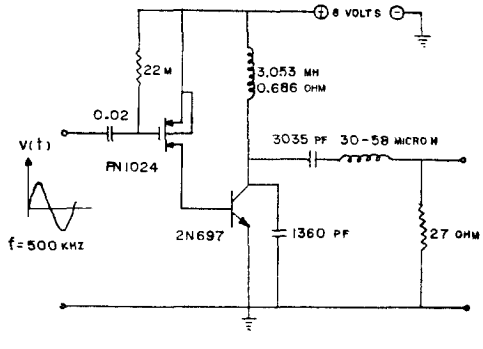


Fig. 5 Illustrative Hybrid Circuit Model

given in the reference. The FET in the input circtit is chosen by considering the following required and preferred conditions.

For this circuit to be excited by a sinusoidal input voltage, which is the most easily obtained wave form, the transistor TR1 should be an enhancement mode FET, preferably one which has high transconductance g_{fs} and has output characteristics giving a steep-edged drain current wave form of about 180 degrees of the input signal cycle (4). The current rating of TR1 must be large enough so that it can provide TR2 with sufficient base current to achieve saturation. The reverse breakdown voltage and transconductance must also be large to give this current saturation condition. For this particular circuit configuration shown in figure 5, TR1 must be a P-channel device.

The selection of TR2 was done primarily in accordance with the conditions specified in the reference. In addition to these critical operating conditions required by TR2, it is desirable to have a high β for higher overall dc to ac power conversion efficiency of the stage.

The above mentioned criteria are met for both transistors used by the author; a p-channel enhancement mode MOSFET FN 1024, and a 2N697 NPN switching transistor. This circuit was built and tested in the laboratory. Figure 6 shows an oscillogram taken from an oscilloscope type AN/USM-140 equipped with a dual trace feature having 10 megohm-10 picofarad probes. From this figure, the peak load voltage V_L is found to be 6 volts. The peak collector voltage across TR2 is 22 volts which is well below the measured BV_{cE} of about 35 volts. The measured dc current with 8 volts V_{cc} was 90 milliamperes, giving the total dc input power of 720 milliwatts. The power dissipated in the RFC is given by

$$P_{RFC}=(90\times10^{-3})^2\times0.686$$
$$=5.55\text{milliwatts.}$$

Therefore, the actual input power to the collector circuit is 714.5 milliwatts. The peak load current I_L is

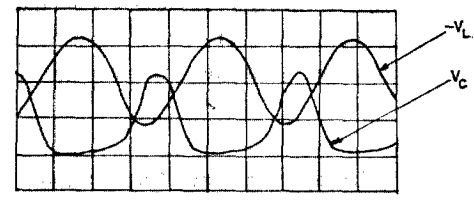
$$I_L=\frac{6}{27}=0.222 \text{ amperes.}$$

The ac power delivered to the load P_L is

$$P_L=\frac{V_LI_L}{2}=\frac{6\times22}{2}=666 \text{ milliwatts.}$$

Neglecting the power lost in the distributed resistance of inductor L and capacitor C, the collector efficiency of the amplifier is calculated to be approximately

$$\text{eff.}=\frac{666}{714.5}=0.932 \text{ or } 93.2\%$$



$-V_L$ = 5 VOLTS/DIVISION, 0.5 MICROSECONDS / DIVISION

V_C = 10 VOLTS/ DIVISION, 0.5 MICROSECONDS / DIVISION

Fig. 6. Oscillogram of Inverted Load Voltage $-V_L$ and Collector Voltage V_C

To see the advantage of the MOSFET in the input circuit, the excitation voltage and current were monitored. An *HP* 650-A test oscillator was used as a sinusoidal source. The peak excitation voltage E_g was 9 volts and the dc gate current flowing would not deflect a 100 microampere full scale ammeter, therefor the excitation power is negligibly small compared to the output power. This very high input impedance excitation stage suggests the possibliity of using a tuned input circuit configuration. The dc power supplied to the FET was 4 milliamperes at 8 volts or 32 milliwatts. Therefore the overall stage dc-to-ac conversion efficiency is approximately

$$\text{eff.}=\frac{666}{720+32}=0.885 \text{ or } 88.5\%.$$

This overall effciency can be further improved by proper choice of devices, TR1 and TR2, and circuit component values. Among other things, the ratio of saturation resistance of TR2 to load resistance must be kept small (4). In this illus-

trative circuit the measured saturation resistance of TR2 was 9 ohm at an I_p of 200 milliamperes. There are many switching transistors commercially available today which have saturation resistances, at the same I_p, of a fraction of an ohm. This effect of the relatively large R_S of this illustrative circuit appears in the oscillogram of figure 6 as a noticeable voltage drop across the transistor during the conduction period of the signal cycle.

If a larger β trasistor isselected for TR2, a lower current rating FET can be used which, at the same time, promotes overall stage efficiency.

V. Discussion and Conclusion

In an r-f power amplifier circuit, the unipolar field effect trasistors possess several advantages over conventional bipolar transistors. The extremely high input impedance characteristic of FETs makes the excitation power required negligibly small, thereby enhancing overall conversion efficiency. The enhancement MOSFET can provide class C operation without biasing, which also improves circuit efficiency.

The low drain efficiency obtained from the illustrative pulse-excited r-f power amplifier circuit is primarily due to the large saturation resistance of the device which was available to the writer. Therefore, by employing the FET which has very low saturation resistance an r-f power amplifier circuit whose conversion efficiency is higher than those of conventional class C amplifier can be built.

The most efficient utilization of the transistors in an r-f power amplifier circuit is found in the hybrid circuit application of the unipolar insulated-gate field effect transistor and the bipolar high-efficiency switching transistor. The extremely high collector efficiency of the conventional switching-mode transistor r-f power generator when excited by a high input impedance MOSFET exciter, can enhance the overall stage efficiency with negligibly small exciting power. By choosing a high f_T, high β, low R_S switching transistor and a high transconductance insulated-gate field effect transistor combination an r-f power amplifier circuit with very high dc-to-ac conversion efficiency can be designed.

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