Master of Science

Al_2O_3를 이용한 MOSCAP 분석 및 원자증착된 고유 전율 Oxide 층을 이용한 AlGaN/GaN MOSHEMT 최적화에 관한 연구

Study on Al_2O_3 MOSCAP and Optimization of Atomic Layer Deposited High-k Oxides for AlGaN/GaN MOSHEMT

The Graduate School

of the University of Ulsan

School of Electrical, Electronic and Computer Engineering

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ABSTRACT

In this thesis, at first an investigation was performed on the properties of atomic-layer-deposited aluminum oxide (Al_2O_3) on an n-type silicon (n-Si) substrate based on the effect of post-deposition heat treatment, which was speckled according to ambient temperature and treatment applied time. Then, making one step ahead, AlGaN/GaN MOSHEMTs and HEMTs grown on Sapphire substrate were successfully fabricated. Various DC characteristics were extracted. The AlGaN/GaN HEMT suffers from high leakage current and self-heating problem. In order to solve this problem, several combinations of Al_2O_3 and HfO_2 gate dielectrics were applied to the device to suppress the high gate leakage current. In every aspect, the MOSHEMTs have given better performance and all the process conditions along with characteristics are discussed briefly with proper reasoning. So far, in MOSHEMT, single Al_2O_3 and HfO_2 have been widely used as gate dielectric whereas their combination can serve better. The optimization of MOSHEMTs by examining various combinations of Al_2O_3 and HfO_2 nanolaminates and their bilayer is the main goal here.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1: Introduction

The purpose of this chapter is to illustrate a framework and introduction of the research work. The whole chapter is divided among some sections which includes research background, motivations, and thesis organization.

1.1 The Scaling

Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is considered as the heart of today's Integrated Circuit (IC) industry. Since from the invention of Integrated Circuit in 1959 by Jack Kilby and Robert Noyce, the evolution of this IC industry has changed our lives meaningfully by the accomplishment of CMOS (a combination of two distinct types of MOSFET named as n-MOSFET and p-MOSFET) scaling [1]. From our personal computer with the microprocessor to recent mobile devices having SoC, the scaling of MOSFET drives the VLSI technology through the increased current density and computing speed as well as lowering power consumption.

Though MOSFET was first proposed and patented in 1930 by J.E. Lilienfield, Kahng and Atalla first reported it on silicon surface after 30 years [2,3]. However, in 1965 Gorden Moore, one of the co-founders of Intel, predicted that the transistor number on a single chip would twofold within every 18-24 months, which is known as the famous "Moore's Law" [4,5] and illustrated in Figure 1.1. Since then it is the guiding principle in the semiconductor industry. Moreover, in 1972, R. Dennard of IBM proposed a set of principles for the scaling purpose of MOS transistors and integrated circuits to smaller dimension [6]. His suggestion was that higher operating speed and reduction in power consumption, as well as lower manufacturing cost through the fabrication of more transistor on a single chip, could be achieved by scaling the physical dimensions of a MOS device. The speed of any MOS device mainly depends on the drive current, which is also known as ON current, and power consumption depends on the off-state leakage current. Succeeding the above-mentioned guideline, two critical properties of MOS device that are channel length (L_g) and gate oxide thickness (t_{ox}) scaled down to about 50 nm and 1.5 nm in early-2000s which were about 4 μm and 50 nm respectively in the mid-1970s [7]. Furthermore, the future required technology for the Semiconductor industry as well as the identified research fields to meet the requirement are governed by an appraisal which is known as "The International Technology Roadmap for Semiconductors (ITRS)" [8]. According to it, after every three years, semiconductor industry implements new technology. Following this roadmap, at 90 nm technology node in 2003, the SiO_2 thickness, which had been conventionally used as gate dielectric material, was only 1.2 nm and the channel length was around 50 nm as well as the strained silicon was used as channel material [8]. In 65 node technology at 2005, the channel length was 40 nm and used second generation silicon technology as channel material and SiO_2 as dielectric. Moreover, Matsushita and Intel introduced 45 nm technology in 2007, where SiO_2 was replaced by a HfO_2 and conventional polysilicon gates were replaced by metal gate [9]. However, these changes failed to meetup the speed and power challenges according to ITRS. In 32 nm technology in 2010, the second generation of metal/high-*k* and fourth generation of strained silicon technology was introduced [10]. In 2012. Intel launched the 22-nm technology which introduced first 3D transistor [11]. Here, the concept of 3-D tri -gate was proposed that forms a channel that abuts three planes in a vertical fin structure. However, form the 14 nm technology and beyond, active research is

going on for new and pioneering materials and device structures for faster speed and low power consumption requirement to continue the CMOS scaling when the gate length is around 10 nm. In addition, when the channel length is compact to 10 nm or less, the traditional channel material which is silicon, is out of the race because of its fundamental material limits and cannot provide performance improvement to continue the scaling. The replacing materials which are now considered are III-V compound semiconductors, germanium, nanowires,2D materials such as graphene and MoS_2 [12]. Among them, III-V semiconductors are now attracted more attention as n-channel materials.

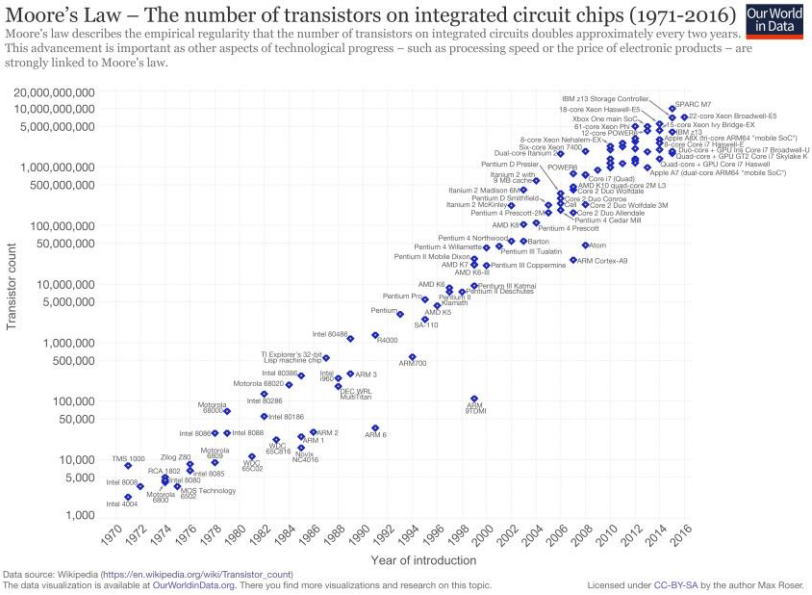

Figure 1.1 Illustration of Moore's law [5].

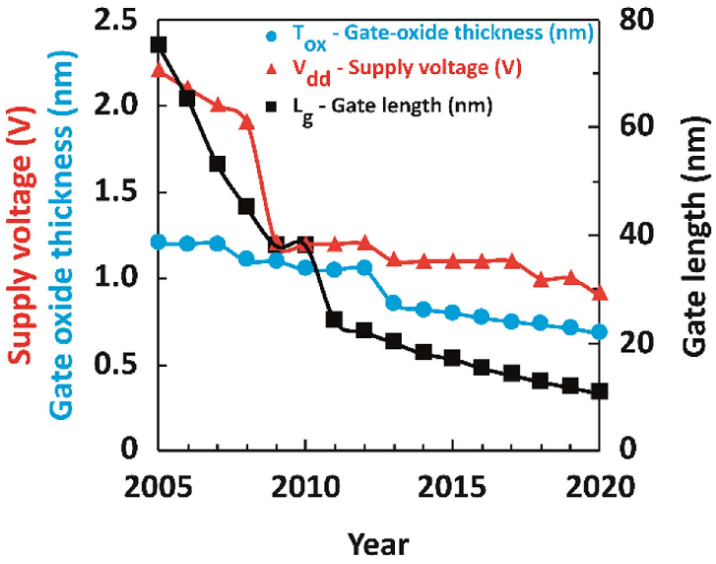

Figure 1.2 International Technology Roadmap for Semiconductors (ITRS) [6].

1.2 The High-k dielectric

Silicon has been a main material of the semiconductor industry over the past several decades. Also, the most important electronic device is the complementary metal-oxide-semiconductor field-effect-transistors (CMOSFETs) made from silicon. One of the key elements that allowed the successful scaling of silicon based CMOSFETs is certainly SiO_2, which has physical and electrical excellent properties as the gate dielectrics. SiO_2 gate dielectrics indeed have several important features that have allowed its use as gate insulator; 1) Amorphous SiO_2 can be thermally grown on Si with excellent control in thickness and uniformity, and naturally forms a very stable interface with the Si substrate, with a low density of intrinsic interface defects, with presenting excellent thermal and chemical stability, which can easily integrate the CMOSFETs due to high immunity to endure high temperature annealing over 1100°C. 2) SiO_2 has quite large bandgap (~ 9eV), which results in the excellent electrical isolation properties, such as its large band offset with the conduction band (CB~3.5eV) and valence band (VB~4.4eV) of Si.

The thickness of the SiO_2 layer presently used as the gate dielectric is so thin that the gate leakage current becomes too high due to direct tunneling of electrons through the SiO_2. The simulated gate leakage current was expected to exceed the leakage limit on gate leakage current density, so that high-*k* gate dielectrics became to need to replace SiO_2 as a gate oxide by 2006. This expectation was realized in 2007 when Intel announced the use of Hf-based high-*k* gate dielectrics in 45nm technology node.

Direct tunneling current through gate oxide decreases exponentially with increasing gate oxide thickness. A CMOSFETs is a capacitance-operated device, where the source drain-current (I_{on}) of the FET depends on the gate capacitance as shown in **Figure 1.3.**

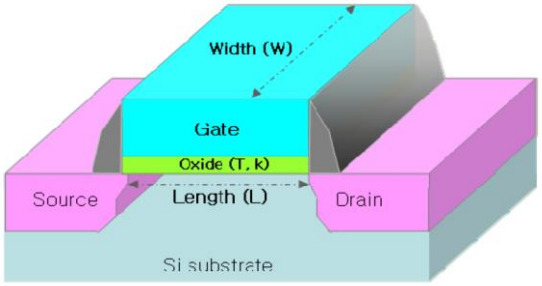

Figure 1.3 The schematic diagram of the field effect transistor (FET)

$$I_{on} = \frac{\mu_{eff} C_{ox,inv}}{2} \frac{W}{L} (V_{gs} - V_{th})^2 \tag{1.1}$$

where I_{on} is the source-drain current of FET, μ_{eff} is the effective mobility of carrier, C_{ox} is the gate capacitance, W and L are the width and length of transistor and V_{gs} and V_{th} are the operating and threshold voltages of transistor. Hence, I_{on} depends on C_{ox}.

$$C_{ox} = \frac{k\varepsilon_0 A}{t} \tag{1.2}$$

where ε_0 is the permittivity of free space, k is the relative permittivity (or dielectric constant), A is the area and t is the oxide thickness. Hence, the solution to the direct tunneling problem is to replace SiO_2 with a physically thicker new material of higher permittivity (k) [13]. This approach keeps the same capacitance or increases the gate capacitance but decreases the gate leakage current. The larger the permittivity of high-k dielectrics becomes, the more the gate leakage current can be decreased. These new gate oxides with high permittivity are called high-k dielectrics. Also, it is convenient to define an electrical thickness of the new gate oxide in terms of its equivalent SiO_2 thickness, or "equivalent oxide thickness" (EOT) as

$$EOT = \frac{3.9\varepsilon_0}{\varepsilon_{high-k}} t_{high-k} = \frac{3.9}{k} t_{high-k} \tag{1.3}$$

where 3.9 is the static dielectric constant of SiO_2 and $t_{high\text{-}k}$ is the physical thickness of high-k oxide. Hence, the most important point is to develop high-k dielectrics which allow scaling to continue to ever lower values of EOT.In this study, another term of EOT, or "capacitance equivalent thickness" (CET) is often used because it can be extracted easily from capacitance values of high-k dielectrics. CET is expressed as

$$CET = \frac{3.9\varepsilon_0 A}{C_m} \tag{1.4}$$

where C_m is the maximum capacitance value under accumulation condition of carrier and A is the area of capacitance. Also, CET is the sum of EOT and any quantum mechanical (QM) effects (0.3~0.4nm), which means EOT equals CET minus 0.3~0.4 nm as shown in **Figure 1.4.**

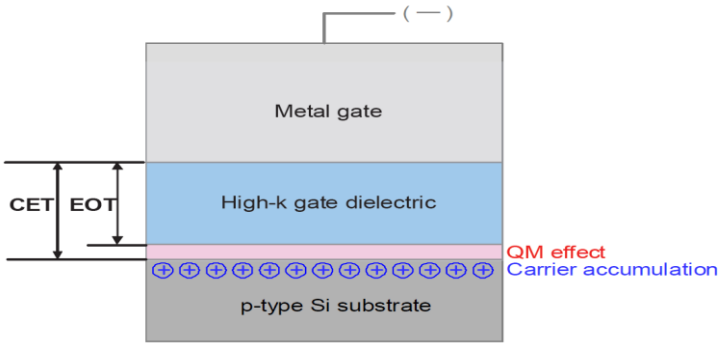

Figure 1.4 The schematic diagram of the capacitance equivalent thickness (CET) and equivalent oxide thickness (EOT)

1.2.1 Selection of high-k gate dielectrics

As mentioned above, the solution to the direct tunnelling problem is to replace the SiO_2 layer with a physically thicker layer of new material of higher dielectric constant (k). These new gate oxides are called high-k gate dielectrics, which are chosen from a large part of the Periodic Table. The new high-k gate dielectrics have to meet several requirements as follows [13]

1. Its k value must be high enough to be used for a reasonable number of years of scaling.
2. The oxide is in direct contact with the Si channel, so it must be thermodynamically stable with it.
3. It must be kinetically stable and be compatible to processing to 1000 °C for 5 s (in present gate first process flows).

4. It must act as an insulator, by having band offsets with Si of over 1 eV to minimize carrier injection into its bands.
5. It must form a good electrical interface with Si.
6. It must have few bulk electrically active defects.

Among these requirements, several important factors are so critical that they have to be fully understood before adopting the high-*k* materials in CMOS applications. Firstly, the relative dielectric constant of the new materials should be somewhere between 12 and 30. There is a trade off with the band offset condition, which requires a reasonably large band gap. The band offset between the gate oxide and Si defines the potential barrier for Schottky injection of electrons or holes into the oxide bands. The potential barrier at each band must be over 1 eV in order to give an adequately low gate leakage current [14, 15]. **Table 1.1** and **Figure 1.5** show static dielectric constants and band offset values, respectively, of the several candidate gate dielectrics, calculated by Robertson [14]. Conduction band offset (CBO) of most high-*k* dielectrics tends to be the smaller than valence band offset (VBO), which means the CBO is one of the key criteria for selecting the new high-*k* dielectrics. Also, the correlation graph between the dielectric constants and the CBO values of the several candidate gate dielectrics is shown in **Figure 1.6.** There is an inverse relationship between dielectric constant and band gap, or band offset. In the graph, there are several oxides with large dielectric constants, such as TiO_2 and $SrTiO_3$, which are candidates for dielectrics in DRAM capacitors [16], but these oxides have a too low CBO as well as low band gap to select the gate oxides.

Table 1.1 Static dielectric constant (*k*) of the several candidate gate dielectrics

Material	Dielectric Constant (*k*)	Band gap E_g (eV)	ΔE_C (eV) to Si	Crystal structure (s)
SiO_2	3.9	8.9	3.5	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.8	Amorphous
Y_2O_3	15	5.6	2.3	Cubic
La_2O_3	30	4.3	2.3	Hexagonal, Cubic
Ta_2O_5	26	4.5	1-1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetragonal
HfO_2	25	5.8	1.5	Mono., Tetra., Cubic
ZrO_2	25	5.7	1.4	Mono., Tetra., Cubic

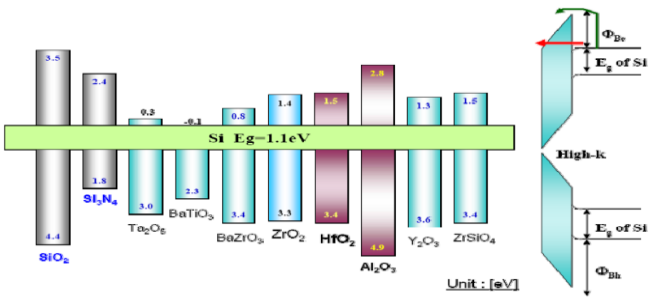

Figure 1.5 Schematic diagram of the band offset values of the several candidate gate dielectrics compared to that of SiO_2

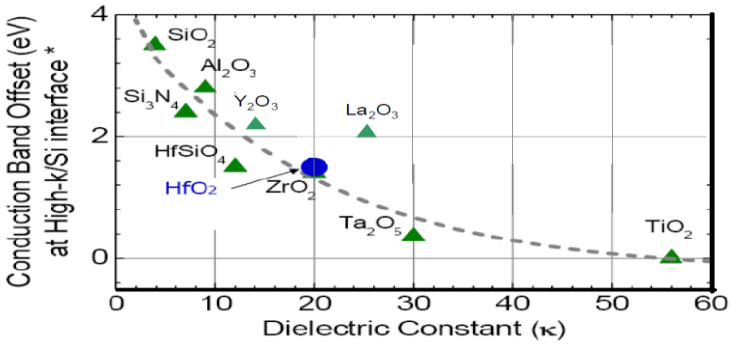

Figure 1.6 Correlation graph between the dielectric constants and the conduction band offset values of the several candidate gate dielectrics

Secondly, the high-*k* dielectrics to use the gate oxide need to have thermodynamic stability. The high-*k* oxides must not react with Si substrate to form either SiO_2 or a silicide according to the unbalanced reactions ($MO_2 + Si = M + SiO_2$ or $MO_2 + 2Si = MSi + SiO_2$). The formation of SiO_2 or un pretended silicide between the oxides and Si would increase the EOT. Therefore, the high-*k* dielectrics should have a large Gibbs free energy of formation to prevent the reactions. **Figure 1.7** show Gibbs free energy as a function of temperature for the oxide formation of the several candidate gate dielectrics [17]. Although SiO_2 have very high thermodynamic stability, there are various high-k dielectrics to have higher formation energy than SiO_2, which indicates that the higher formation energy of several high-*k* dielectrics suppresses the unbalanced reaction. Moreover, oxygen diffusion coefficients must be low because they will cause uncontrolled interfacial layer regrowth.

Finally, the high-k dielectrics must form a good electrical interface with Si, because the oxides are in direct contact with the Si channel. The carriers in the channel flow within angstroms of the interface between the oxide and Si. Hence, this interface must be of the highest electrical quality. In other word, low interface trap defect density, D_{it}, typically less than ~ 10^{11} $cm^{-1}eV^{-1}$ is required.

To satisfy these various requirements for selecting new high-k dielectrics, various kinds of high-k gate dielectrics such as Al_2O_3, Ta_2O_5, ZrO_2, HfO_2, TiO_2, La_2O_3, and many others have been widely investigated for the past decade. Ta_2O_5, TiO_2 and Al_2O_3 as new gate dielectrics had been studied in the early days due to their maturity in memory capacitor applications. However, these materials except Al_2O_3 are not thermodynamically stable in direct contact with Si. In addition, TiO_2 and Ta_2O_5 have a relatively low conduction band offset with silicon, which can lead to increase electron tunnelling currents [14]. In the case of Al_2O_3, its dielectric constant (~9) was not enough to satisfy the requirement of high-k gate dielectrics although it has superior thermodynamic and kinetic stability. Considering proper dielectric constant and large band gap and high thermochemical stability, Hf and Zr-based high-*k* dielectrics including their silicates mush have been the leading candidates.

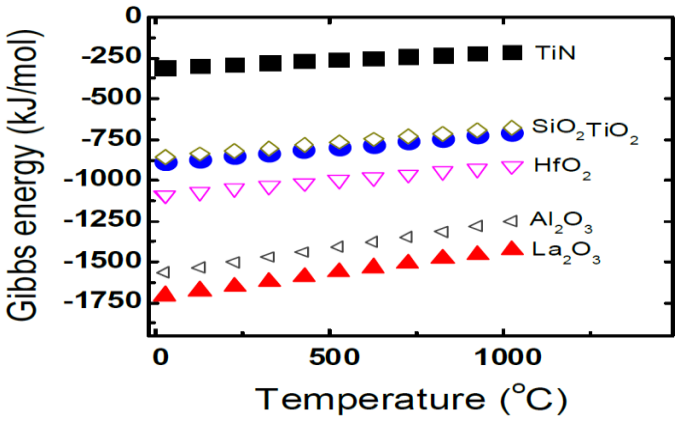

Figure 1.7 Gibbs free energy for the oxide formation of the several candidate gate dielectrics as a function of temperature [17].

1.3 The Metal Gate

As mentioned earlier, one of the key elements that allowed the successful scaling of silicon based CMOSFETs is certainly SiO_2. Like SiO_2 gate oxide on Si substrate, poly-Si gate electrode on SiO_2 gate oxide is another key element that allowed the superior improvement of transistor's performance and the easy integration of CMOS process. The purpose of the gate electrode in CMOS is to shift the surface Fermi (E_f) of the Si channel to the appropriate band edge. An NMOS transistor consists of a p-doped Si channel and its gate electrode with low work function (~ 4.05eV) will move E_f at the channel surface to its conduction band. A PMOS transistor has a n-doped Si channel and its gate electrode with 5.15eV will shift E_f into its valence band. A difference in work function (WF) of gate electrodes is almost 1.1eV, or the Si band gap.

In CMOSFETs used above 45nm technology node, the gate electrodes are polycrystalline Si doped highly n-type or p-type, respectively, for NMOS and PMOS. Their WFs of n- and p-type doped poly Si gates are usually 4.05eV and 5.15eV, respectively. The doped poly-Si material has the advantage that it is refractory, easily deposited and doped, and compatible with SiO_2 and the process flows. Especially, the controllability of the WF through implantation of dopants has facilitated the easy adjustment of threshold voltage of CMOSFETs.

However, need for metal gates in next-generation scaled CMOS devices was firstly discussed by an early paper which was published in International Electron Devices Meeting 1997. As CMOS devices were scaling down to sub-micron technology node, poly-Si gate electrode used generally in conventional CMOSFETs was faced with several critical issues such as poly-Si gate depletion, boron penetration and high gate resistance. Doped poly-Si gate electrode has limited carrier density, and so it contributes a depletion length of order 0.2nm to the capacitance equivalent thickness (CET) of the gate stack. Also, the penetration of doping element, especially boron, into Si channel through the gate oxide has deteriorated reliability of CMOSFETs. At an introduction of high-k gate dielectrics, poly-Si gate electrode has been found to be fundamentally incompatible with ZrO_2 or HfO_2 oxide. It was found that the reducing ambient during the CVD deposition poly-Si from silane causes a gross reduction of the ZrO_2 or HfO_2, leading to silicide formation, leakage paths, Hf–Si bonds and nuclei for the

large grain poly-Si growth [18, 19]. Therefore, high-k gate oxides and metal gates must to be introduced simultaneously.

The gate metals to be used must to be 'band edge metals', with WFs equal to the band edge energies of Si, 4.05 and 5.15 eV. Also, the gate metals must to have the thermal stability of that metal in contact with the gate oxide and the process compatibility such as etch. Although replacement of the poly-Si gate electrode with the metal gate has been already implemented below 45nm technology node, there are still several issues. For example, NMOS metals with small WF are too reactive and unstable to maintain the low WF, while PMOS metals with high WF are too noble and difficult to etch.

1.4 The III-V Materials

High mobility materials, such as III-V compound and Ge semiconductors, have shown promise for future high-speed and low power applications. **Figure 1.8** shows materials for "More Moore" diversification towards III-V logic applications [20]. **Table 1.2** shows properties of Si, Ge, and the prominent III-V semiconductor compound substrates, including effective mass (e*), energy gap (E_g), electron and hole mobility (μ_e and μ_h, respectively), and saturation velocity (v_{sat}). Materials such as GaN, InGaAs, InAs, and InSb have superior characteristics in terms of these properties that makes them promising candidates for low noise, low power, and high-speed digital applications for n-type channel devices. Furthermore, they have flexibility to be band-engineered. For example, InAs has electron mobility as high as 33,000 cm^2/Vs. In combination with InGaAs, mobility and peak saturation velocity can thus be improved. In addition, InSb, GaSb, and various Sb-based alloys have high electron and hole mobilities and can be strained to be utilized in p-channel III-V logic applications [21,22].

Table 1.2 Principal Material Properties of Si, Ge, and III - V Semiconductor Compounds [20]

Property	Si	Ge	GaN	$In_{0.53}Ga_{0.47}As$	InP	GaAs
$e^*(m^*/m_0)$	0.19	0.082	0.067	0.041	0.077	0.067
E_g (eV)	1.12	0.66	3.39	0.74	1.35	1.42
μ_e (cm^2/Vs)	1,350	3,900	1,000	12,000	4,600	8,500
μ_h (cm^2/Vs)	450	1900	200	300	150	400
v_{sat} ($\times 10^7 cm/s$)	1	0.6	1.4	3.1	2.5	2.1

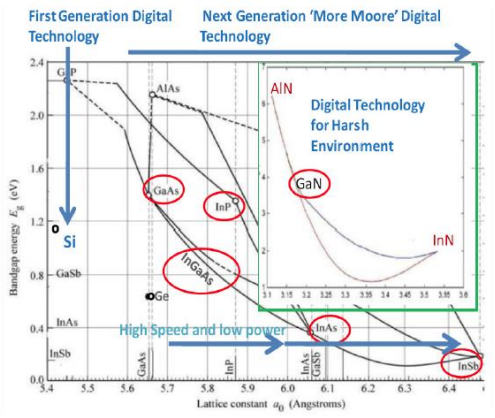

Figure 1.8 Diversity of III-V materials that can be used for logic applications compared to Si and Ge [20].

There are a wide range of III-V compounds and they have low effective masses, which gives rise to high injection velocities. Their lower density of states, comparing to Si, yield less scattering, but limits achievable carrier densities. Higher mobilities also give lower access resistance. These superior transport properties paired with smaller bandgaps result in higher speed MOSFET performance. As for more performance per gate width, having more current requires less applied bias, which in turn reduce power consumption. In addition, higher performance decrease FET widths, which reduces IC overall size. Structurally, III-V compounds can be engineered to have strong heterojunction properties such as large band offsets, which give rise to better carrier confinement, decreasing leakage current issues in the devices.

AlGaN/GaN high-electron-mobility transistors (HEMTs) have been developed for high-power and high-frequency applications because of their excellent properties, such as high electron mobility of two-dimensional electron gas (2-DEG) channel, high breakdown field, and wide energy bandgap [23]. Although AlGaN/GaN HEMTs have high commercial applications in high-frequency power amplifier industries, the conventional Schottky-gate HEMTs suffer from large gate leakage current [24], which limits the output power performance and induces reliability issues [25]. Therefore, AlGaN/GaN metal-insulator-semiconductor-HEMTs (MIS-HEMTs) that employ MIS gate insulators would be good alternatives for reducing the gate leakage current [26] and increasing the breakdown voltage [27-29]. Superior DC and RF characteristics in comparison with the conventional Schottky-gate HEMTs have been reported by using various insulators for AlGaN/GaN MOS-HEMTs, such as SiO_2 [30], SiNx [31], Al2O3 [32], HfO2 [33], and Sc2O3 [34], etc. However, a drawback of the AlGaN/GaN MIS-HEMT is the low transconductance (gm) that is caused by the increase in the effective barrier thickness [35], which limits the performance. A possible solution can be achieved by the use of a AlGaN/GaN MOS-HEMT structure in conjunction with a thin gate insulator, where the gate region was recessed to enhance the gm. [36] However, the gate recess configuration results in a reduced 2-DEGchannel concentration and, thus, limits the output current density and RF performance. Therefore, the trade-off relationship must be carefully considered while employing the recessed MOS gate structure. However, one of the key problems limiting the performance and reliability of AlGaN/GaN HEMTs for high-power RF applications is the high Schottky-gate leakage current [22], which results in the degradation of DC/RF parameters [23]. At positive gate bias, high forward gate current can shunt the gate-channel capacitance, thus limiting the maximum drain current. At negative gate bias, high voltage drops between the gate and drain resulting in premature breakdown and the maximum applied drain voltage is restricted. Besides, gate leakage current increase resulting in the device sub-threshold currents, which decrease the achievable amplitude of RF output. All these limitations become the most important key factors to be solved for the development of the advanced wireless communication system [25].

To overcome this problem, several groups have been trying to integrate the MOS structure into conventional Schottky-gate HEMT by looking for proper gate oxides for AlGaN/GaN based HEMT. Al2O3 has been used as the dielectric gate to reduce the gate leakage, which allows the application of high positive gate voltage to further increase the sheet electron density in 2D channel [25].

1.5 Motivation

To understand III-V compound semiconductors used to fabricate MOSHEMTs, there are many technological challenges need to be conquered. One of the main obstacles is the gate dielectrics which lack high oxide quality, thermodynamic stabilization, low leakage current, high breakdown fields ,and excellent native oxide like SiO_2 on Si naturally .Moreover, III-V surface exists such as vacancies, defects, or incomplete dimerization which cause unsaturated bond sand form electrically active traps [37,38].Thus, high interface trap densities might give rise to insufficient Fermi-level response, preventing control over the charge carriers in the channel[39], the degradation of the drive current, and the subthreshold swing. For that reason, the interfacial control in III-V gate stack is strongly needed for realizing low D_{it}. To develop appropriate gate dielectrics and better interface properties, forming a stable interface with suitable thermal budget and how to reduce the density of interface states (D_{it}) are the important issues. In particular, fabricating good interface qualities between III-V and high-*k* dielectrics are extremely challenging. Also, the traps in the oxide itself which are located near the interface as known as border traps make a dispersion in the capacitance-voltage response. However, th e effect of these near-interfacial dielectric traps is a great stimulus for the on-state act of a MOSFET. Because the Fermi level (E_f) is pinned inside the conduction band, border traps prevent the formation of sufficient carriers in the channel, which leads to reduced c arrier mobility by phonon scattering and eccentricity of the threshold voltage [40,41].The impact of border traps is more prominent in the accumulation region, where a dispersion is always observed in the capacitance-voltage (C-V) response of the metal- oxide-semico nductor(MOS) capacitor because of the transportable carrier exchange among the border traps and conduction band states via tunneling, as described previously [42-45]. To understand the device behavior properly the characterization of these traps according to device response is necessary. In this work, the trap characterization, reliability, and current-voltage properties will be analyzed of the MOSHEMTs using Al_2O_3 and its nanolaminates according to the Al doping concentration into HfO_2 as well as deposition parameter. Besides that, gate capacitance modelling and overall device performance will also be focused.

1.6. Thesis organization

This thesis is structured to illustrate the theoretical and experimental presentation of the research conducted by the author. In detail, the fabrications of MOSHEMTs with Al_2O_3 and HfO_2, and their bilayer (Al_2O_3/HfO_2) as well as nanolaminate (HfAlO) structure and their DC characteristics as well as trap characteristics (D_{it} and N_{bt}) were analyzed. The thesis is organized as follows;

- Chapter 1. Introduction

  A short introduction and motivation behind the study, and overall works contents are illustrated in this section.

- Chapter 2. Literature review and background

  Backgrounds of this study along with nanomaterials familiarization and the

state of the art are discussed elaborately in this section

- Chapter 3. A brief study on the effects of post-deposition annealing for ALD-deposited Al_2O_3 on an n-type silicon substrate.

- Chapter 4. Optimization of atomic layer deposited high-k oxides for AlGaN/GaN MOSHEMT.

- Chapter 6. Conclusions and future work

  The overall outcomes of this research are summarized in this section. Furthermore, some suggestions for the improvement of this model was also analyzed for the future work related to this research are discussed.

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CHAPTER 2: Literature and Background Review

2.1 Metal-Oxide-Semiconductor structures (MOS)

Metal-Oxide-Silicon (MOS) capacitor is the basic structure used in silicon FET to control the conductive channel by gate bias. **Figure 2.1** shows the cross-sectional view of a MOS capacitor, where V_G is the applied gate voltage. For an ideal MOS capacitor, both the oxide and the oxide- semiconductor interface are assumed to be free of charges and defect states. Depending on the polarity and magnitude of the applied gate voltage, the carrier concentration and band structure of semiconductor changes resulting in different electrical characteristics of the MOS capacitor.

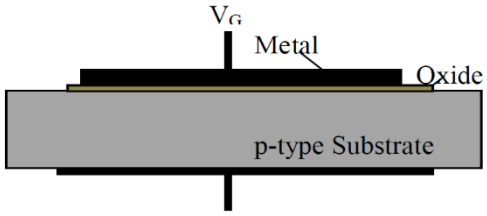

Figure 2.1 Schematic diagram of MOS Capacitor

A MOS structure with Φ_{MS}, which is the work function difference between metal and semiconductor is zero and no interface and mobile charges in the oxide is called an ideal MOS capacitor. **Figure 2.2** shows the energy band diagram of an ideal MOS capacitor, with p type semiconductor at thermal equilibrium (V_G=0). Φ_M-metal work function, χ_i-electron affinity of the insulator, χ-electron affinity of semiconductor, E_g-energy gap of semiconductor, Φ_B-potential difference between the metal Fermi level and conduction band of the insulator, Ψ_B-potential difference between the intrinsic Fermi level (E_i) and Fermi level (E_F) inside the bulk, E_C-conduction band edge and E_V-valance band edge of the semiconductor. These energy barriers prevent the free flow of carriers from the metal to the silicon or vice versa. Thus, the application of a bias across the MOS capacitor does not result in current flow. Rather, an electric field is established in the oxide by surface charge layers that form in the metal and on the silicon-oxide interface [1-3].

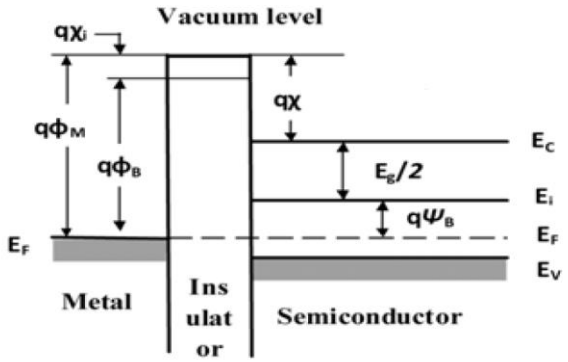

Figure 2.2 Energy-Band diagram of ideal MOS structure in thermal equilibrium constructed from a p-type semiconductor substrate.

For an ideal MOS system, when the applied gate voltage $V_G = 0$ the energy bands are flat and known as flat band condition. From **Figure 2.2**, the work function difference can be written as follows [2,3]

$$\phi_{ms} = \phi_m - \phi_s = \phi_m - (\chi + \frac{E_g}{2q} - \psi_B) = 0 \tag{2.1}$$

where Ψ_B is negative for p-type and positive for n-type substrates. When a gate voltage $V_G \neq 0$ is applied to an ideal MOS structure, the charges are distributed at the semiconductor-insulator or metal-insulator interface with equal amount and opposite polarities. It is assumed that under applied gate voltage V_G, there is no charge transfer throughout the insulator, which means that it has an infinite resistance. Depending on the polarity and magnitude of the gate voltage, the MOS can control the type and value of the current through MOSFET channel. There are mainly three working regions for a MOS capacitor depending upon whether applied gate voltage is positive or negative.

2.2. Capacitance-Voltage (C-V) analysis of MOS capacitors

C-V analysis is considered as one of the most important tools for characterizing MOS systems [1]. In this the differential capacitance is the most essential property, because small-signal measurements determine the changing rate of the charge with voltage. To understand capacitance-voltage measurements properly one must first be familiar with its frequency dependence. The frequency dependence occurs primarily in inversion region, since a certain time is needed to generate the minority carriers in the inversion layer. High and low frequency C-V measurements are often useful among various methods to evaluate the MOS characteristics. Most of the capacitance measurements are performed with admittance bridges or capacitance meters. By applying Gauss' law, the small-signal equivalent circuit of the MOS capacitor was derived as follows [1,2]:

$$\frac{1}{C} = \frac{1}{C_S(\psi_S)} + \frac{1}{C_{ox}} \tag{2.2}$$

Equation 2.2 gives the total capacitance of the MOS device as the sum of the silicon capacitance and the oxide capacitance, per unit area in series. The majority and minority carrier response times to ac gate voltages are different. The minority carrier response time is typically as long as 0.01-1s, which is much slower than the frequency of bias at high frequency and hence certainly not instantaneous over the frequency range of interest. **Figure 2.3** clearly shows the ideal C-V characteristics of a MOS capacitor with accumulation, depletion and inversion region. Normalized capacitance value is maximum at accumulation region and equal to the oxide capacitance. For the depletion region, as the silicon capacitance increases by the formation of the depletion layer, the total capacitance decreases as they are in series with each other. Finally, for the inversion region total capacitance is the series combination of oxide capacitance and inversion layer capacitance. Depending upon the frequency of the ac voltage applied it is possible to observe two different behaviours. First, if the frequency is low enough, minority carrier generation takes place efficiently and electrons form an inversion layer at the oxide-silicon interface [1]. Therefore, the total capacitance increases and reaches back to its maximum value for positive gate voltages. Second, if the applied frequency is high enough

(1MHz) then the minority carriers cannot be generated fast enough and hence cannot form an inversion layer at the oxide-silicon interface. In this case, the capacitance reaches its minimum value and stays constant even if the applied gate voltage is increased to higher positive values.

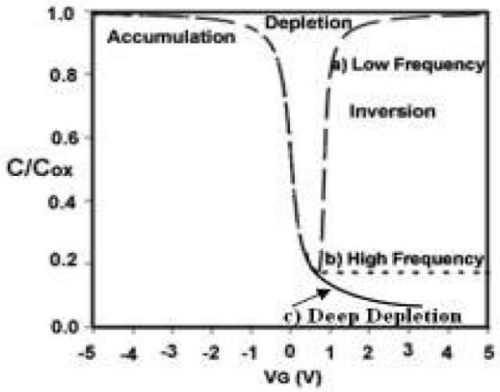

Figure 2.3 Ideal C-V curve for a MOS capacitor (a) low frequency (b) high frequency (c) deep depletion

Usually C-V curve is measured by automatically sweeping gate bias. If sweep rate is too rapid for minority carriers to follow, the system no longer wills be in thermal equilibrium with respect to gate bias and resulting C-V curve will differ from thermal equilibrium curve. At room temperature, the minority carrier generation rate will be much smaller than the recombination rate. The sweep rates normally used are too rapid for generation to follow but are slow for recombination to follow. At room temperature the system usually is not in equilibrium when gate bias is swept in the direction of increasing inversion, but it is in equilibrium when gate bias is swept in the direction of decreasing inversion. If response is too slow for minority carriers to follow the gate bias sweep into inversion, no inversion layer forms. Therefore, the charge neutrality must be satisfied by increasing the width of depletion layer wider than the thermal equilibrium and under this condition the capacitance decreases below its thermal equilibrium saturation value. This non-equilibrium condition is known as deep depletion [1].

2.3 Non-ideal Effects

In actual MOS capacitors, there are several non-ideal effects that may result in deviation from ideal behaviour. The work function difference between the metal and semiconductor due to variation in the doping level of semiconductor material is one such cause of non-ideal effect. To compensate this work function difference an external voltage should be applied to the MOS structure. For this bias condition, the energy bands of Si are flat up to the interface and do not vary with distance. This applied voltage to achieve flat band condition is called the flat band voltage and is represented by V_{FB} for the MOS capacitor. If the oxide material does not contain any oxide or interface trap charge. The V_{FB} can be written as.

$$V_{FB} = \phi_{ms} = \phi_m - (\chi + \frac{E_g}{e} - \phi_P) \tag{2.3}$$

where Φ_m-metal gate work function, Φ_s-semiconductor work function, χ-semiconductor electron affinity, E_g-semiconductor energy gap, and Φ_p-position of semiconductor Fermi level above the valance band in the neutral semiconductor bulk. The difference in work functions

represents the amount of band bending. The sign of the difference of the metal and semiconductor work functions gives the polarity of applied voltage to be connected to the metal to obtain the flat band condition.

Other non-ideal effects are mainly due to charges present in the oxide and at the semiconductor-oxide interface. It has been established that there are mainly four general types of charges associated with the oxide/Si system as summarized in **Figure 2.4**. The total charge per unit area is represented by Q (C/cm^2) and the number of charges per unit area (the number density) is represented by the symbol N ($number/cm^2$).

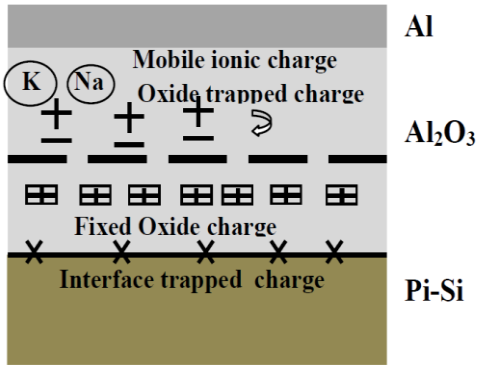

Figure 2.4: Various charges present in MOS structures.

The first type of charge is named as the fixed oxide charge Q_f which is primarily due to the structural defects (such as ionized silicon) in the oxide layer. The density of this type of charge is closely related to the oxidation process. **Figure 2.5** shows a comparison of the energy band diagrams for ideal n and p type MOS structure. For these ideal structures, at zero applied voltage on the metal gate, it is a state of flat band. However, because of the difference between the gate metal work function (Φ_m), and the semiconductor work function (Φ_s) many dielectrics exhibit a charge at the silicon surface resulting in a required applied voltage $V_{FB} \neq 0$ to achieve a flat band condition.

The simplest and most widely used method for measuring oxide charge density N_{eff} is to infer this density from the voltage shift of C-V curves, caused by the existence of oxide charges, as shown in the right part of **Figure 2.6**. In both cases (p substrate and n substrate) positive Q_f causes the C-V curve to shift to more negative values of gate bias with respect to the ideal C-V curve. If the oxide charge is negative then the entire C-V curve is shifted to more positive value with respect to the ideal C-V curve, and negative oxide charge cause the C-V curve to shift to more positive value with respect to the ideal C-V curve. The bias shift of the C-V curve caused by oxide charge Q can be explained by image charges. Using a n-type substrate as an example, for a certain gate bias without any charge, at depletion region, the ideal depletion layer width is such that negative charge on the gate is balanced by the positive dopant ions in the depletion layer. If positive charge is joined in the oxide as shown in the upper-right side of **Figure. 2.5**, the above charge balance is interrupted, its image charge (actually electrons for this case) is introduced in the silicon substrate. These additional electrons located at the depletion layer, partly neutralize and reduce the depletion layer width. Because the capacitance of Si (C_s) is inverse to the width of the depletion layer and in series connection to C_{ox}, the actual

capacitance with oxide charge Q becomes larger than for the ideal capacitance without Q (**Figure 2.6** right top Figure). At strong accumulation, this influence of image charge is omitted because of the accumulation of carriers at the surface of Si from the substrate and absence of depletion region. At strong inversion, for low frequency measurements capacitance value reaches the same saturation value as in the case of accumulation and hence the effect of image charge is absent.

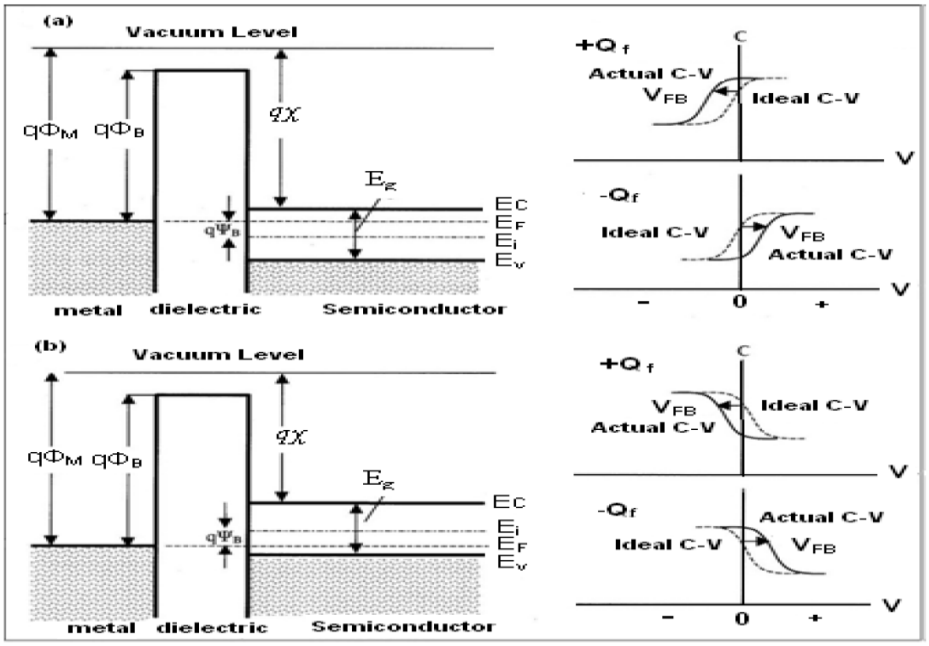

Figure 2.6 Energy-band diagrams and associated high frequency C-V curves for ideal MIS diodes for (a) n-type and (b) p-type semiconductor substrates. For these ideal diodes, $V_G = 0$ corresponds to a flat band condition. For dielectrics with positive (Q_f) or negative ($-Q_f$) fixed charge, an applied voltage (V_{FB}) is required to obtain a flat band condition and the corresponding C-V curve shifts in proportion to the charge in dielectrics.

The second type of charges is the oxide trapped charge, Q_{ot}. These are due to holes or electrons trapped in the bulk of the oxide layer and can arise from the ionizing radiation or avalanche injection. Thus, Q_{ot} can have a positive or a negative value. Third type of charge is called mobile ionic charge, Q_m, which is mainly due to ionic impurities such as Li+, Na+, and K + etc. The sum of these three different charges in the oxide layer is represented by the effective oxide charge Q_{eff} (and its number density N_{eff}) as given in **Equation 2.4**.

$$Q_{eff} = Q_f + Q_m + Q_{ot} \tag{2.4}$$

Finally, the fourth and the most important source of non-ideal effects is due to interface trapped charge Q_{it}. Its density per unit area per unit energy is denoted by D_{it}. They are usually located at the oxide-semiconductor interface. It has a positive or a negative value depending on the location with respect to the Fermi level. They originate from structural disorder, oxidation- induced defects, metal impurities and defects caused by radiation or similar bond-breaking processes. Various techniques like Conductance's method and simultaneous C-V methods are used to calculate the level of interface trap density. D_{it} plays a major role in the operation of MOS devices causing an increased recombination of the free carriers in the conduction and valance bands. The levels of the $Q_{eff\ and}$ D_{it} are the important parameters to be controlled during the manufacturing process of the MOS devices.

2.4. Atomic layer Deposition

An ALD process requires at least two different vapor-phase precursors. In contrast to normal MOCVD process where precursors are introduced into process chamber simultaneously, ALD process breaks the reaction into two half-reactions by leading precursors into process chamber in separate and alternate pulses. During the pulse flowing, the precursors are chemically adsorbed onto the substrate and react with surface groups. Between two adjacent precursor pulses, inert gas normally flows into ALD chamber to purge the precursor residuals and reactant molecules out [4]. Generally, one ALD cycle consists of a pulse of metal precursor and a pulse of oxidant.

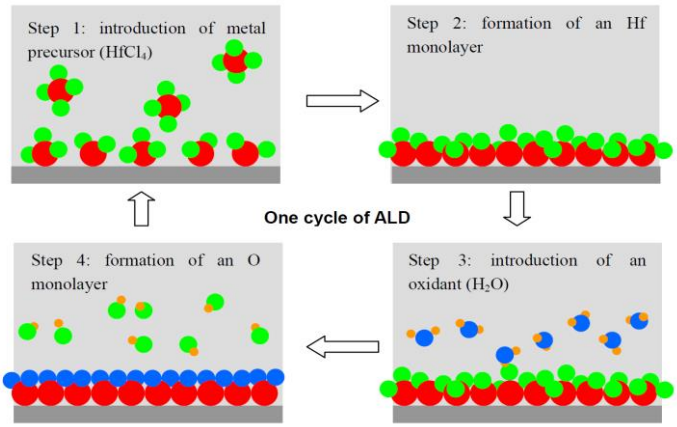

Figure 2.7 A schematic illustration of an-ALD process cycle. By repeating the ALD cycle, the stoichiometric HfO_2 can be deposited.

A standard ALD process cycle can be divided into four steps [5], as schematically illustrated in **Figure 2.7**. Firstly, metal precursor molecules are chemically adsorbed onto the substrate surface during the metal precursor pulse. Secondly, the unabsorbed or unreacted metal precursor molecules are purged away by inert gas. Thirdly, oxidant precursor (H_2O) molecules are exposed to the substrate and react with metal precursor molecules forming desired metal oxide material by generating the volatile by product. Fourthly, the unreacted precursor residues and volatile by products are purged away by inert gas. Thus, by repeating the ALD cycles, thick films are deposited. Theoretically, one ALD cycle deposits a monolayer material. In practice, due to steric hindrances, one ALD cycle usually deposits only a fraction of a monolayer, like half monolayer.

Furthermore, as shown in step 1 and step 3 in **Figure 2.7,** the precursor is reactively adsorbed onto the surface. After the precursor is exposed to a certain extent, all of the surface will be covered by the precursor, then reaction saturates and stops. This is called self-limiting reaction, which is one of the most important characteristics of ALD process [4]. To characterize the self-limiting behaviour, a plot of pulse length *vs.* growth rate is usually used, as shown in **Figure 2.8**. Here, the self-limiting behaviour of HfO_2 deposition is used as an example. When pulse length of $HfCl_4$ precursor is greater than 0.4 s, growth rate of HfO_2 keeps constant and is independent on the precursor pulse length. This region is self-limiting region. With this wide region, the deposition rate can be maintained constantly in different cycles, resulting in a strict linear relationship between the film thickness and the numbers of growth cycle. Thus, by simply varying the cycle numbers, film thickness can be easily and accurately controlled down

to the atomic level [4]. Moreover, the reaction in step 1 and step 3 shown in **Figure 2.7** is a pure surface reaction. The pure surface reaction makes the deposition rate consistent everywhere across the wafer regardless of the surface morphology. Thus, almost perfect step coverage can be achieved. Furthermore, the surface reaction provides better control in dopant distribution [6].

In addition, the purge steps (step 2 and step 4 shown in **Figure 2.7**) separate precursors into different pulses. Thus, the precursors will never meet each other in the gas phase, which eliminate the gas-phase reaction. The elimination of gas-phase reaction greatly reduces the risk of particle formation in gas phase [6]. This is another advantage of ALD process.

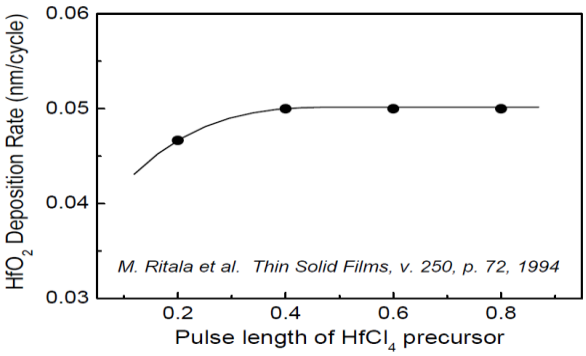

Figure 2.8 A schematic illustration of self-limiting characteristic using ALD HfO_2 as an example [6]. When the pulse length is greater than 0.4 s, the deposition rate is independent of the pulse length, which implies a wide process window to achieve the constant deposition rate.

2.5. Interface Trap Densities (D_{it}) Extraction

High trap densities (D_{it}) at the interface between gate dielectrics and the III-V channel cause inefficient Fermi level response or even Fermi level pinning. Metal-oxide-semiconductors capacitors (MOSCAPs) are normally used for separately addressing the issues with high-k/III-V interface. Methods for analysing D_{it} at the SiO_2/Si interface using MOSCAPs structures were developed in the 1960s [1]. The quantity measured in a MOSCAP is its admittance as a function of gate bias and frequency. However, compared to SiO_2/Si interfaces, the interpretation of the admittance response in high-k/III-V systems is less straight forward. With their variation of band gaps, low conduction band density of states, and wide range minority carrier response times, the methods for D_{it} analysis have to be adjusted. In addition, the energy distribution of the D_{it} also varies. Normally, more than one method is required to compare and contrast the D_{it} values and distributions. In this dissertation, the conductance method is mainly used.

2.5.1 Conductance Method

Measurement of the equivalent parallel conductance can be used to estimate interface trap densities because the conductance is directly related to energy loss provided by AC signal source during capture and emission of carriers by interface traps [1]. The equivalent parallel conductance, G_p, can be extracted by

$$Gp = \frac{\omega^2 C_{ox}{}^2 G_m}{Gm^2 + \omega^2 (\mathrm{C_{ox}} - \mathrm{C_m})^2} \tag{2.5}$$

where ω is the angular frequency (2πf), C_{ox} is the gate oxide capacitance, G_m is the measured conductance, and C_m is the measured capacitance. During the measurement, the occupancy of the interface traps changes as a function of AC signal, which reaches a maximum when the interface traps are at resonance with the applied AC signal (ωτ=1). Consequently, the maximum normalized parallel conductance peak, $(\frac{G_p}{A\omega q})_{\max}$, where A is the device area and q is the elemental charge can be used to estimate D_{it} values

$$D_{it} \approx 2.5(\frac{G_p}{A\omega q})_{\max} \tag{2.6}$$

The estimated D_{it} values are reliable when $C_{ox} > qD_{it}$. When $C_{ox} < qD_{it}$, D_{it} is underestimated because the measured impedance is dominated by C_{ox} [19]. This method assumes a constant capture cross section on the semiconductor surface. Thus, for different semiconductor compounds, the constant capture cross section can vary because of different types of traps and energy levels inside the band gap [20]. The trap energy level can be referred to as the energy difference to the majority carrier band edge (ΔE), which can be estimated from its relationship to the frequency at $(\frac{G_p}{A\omega q})_{\max}$. The frequency dependence is related to the characteristic trap response time, $\tau = 2\pi/\omega$. It describes the time needed for a captured charge to be released by a trapping state at energy level E. The trap response time is given by the Shockley- Read-Hall statistics of capture and emission rates [21,22].

$$\tau = \frac{\exp(\Delta \mathrm{E}/\ \mathrm{k_B T})}{\sigma v_{th} D_{dos}} \tag{2.7}$$

where σ is the capture cross section of the trap, V_{th} the average thermal velocity of the carriers, D_{dos} the effective density of states of the majority carrier band, kB the Boltzmann constant, and T the temperature. CV and conductance-voltage measurements have to be performed at different temperatures in order to extract the D_{it} across the $In_{0:53}Ga_{0:47}As$ bandgap. With the $In_{0:53}Ga_{0:47}As$ parameters taken from ref. [23] and the assumed capture cross section σ of 1 $x10^{-16}$ cm^2, the characteristic trap frequency can be calculated from **Equation 2.7** for different temperatures as a function of energy difference between the majority carrier band. This is shown in Figure 2.11. The frequency range is 100 Hz to 1 MHz. The data for σ of $In_{0.53}Ga_{0.47}As$ is assumed due to the lack of measurement reports. The reported values are in 7 $x10^{-15}$ to 5$x10^{-17}$ cm^2 range [19]. It is noted that errors can appear, but they are expected to be small. Errors arise in low temperature measurements since the D_{it} response is not as pronounced as those at higher temperature. Consequently, the D_{it} values close to the band edges are less reliable compared to those near midgap. The plot indicates that low temperature measurements are required to determine the D_{it} values close to the band edges. Room temperature measurement can only be used for extract the near midgap D_{it} values in this frequency range (< 1 MHz).

2.6. Bulk-Oxide Trap in High-k/III-V MOS Structure

Distributed circuit model is applied in this chapter to explain the C-V and G-V dispersion of MOS capacitors in accumulation region and characterize the bulk-oxide trap density. The

series resistance effect is also introduced by adding an additional resistance component to the model, explaining the well observed upturning G_{tot} at high frequency.

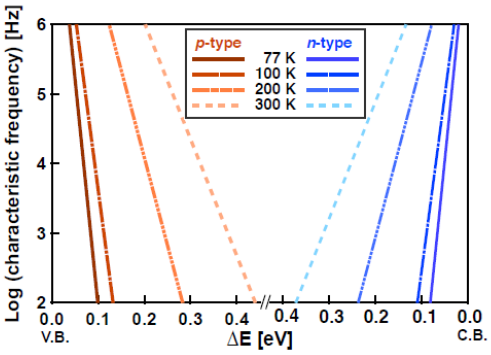

Figure 2.9 Characteristic trap frequency of $In_{0.53}Ga_{0.47}As$ as a function of energy difference between the majority carrier band and the trap energy level

2.6.1 Distributed Bulk-Oxide Trap Model

The Full-interface state model described in previous section has single τ_n and τ_p at given bias, which leads to a high-low type of transition in capacitance dispersion from low to high frequency. It cannot explain the uniform capacitance dispersion data in accumulation. Instead, such uniform dispersion has been explained by the bulk-oxide trap effect [24]. Different from interface traps, bulk-oxide traps are in the bulk dielectrics, and they exchange charges with mobile carriers in the semiconductor through tunneling; therefore, it has relatively large and wide-spreading time constants. The tunneling process in n-type MOS capacitor is schematically illustrated in **Figure 2.10**. In the static picture, consider single-level oxide traps of density N_{bt} (cm^{-3}) at energy E_t, shown schematically in **Figure 2.11.** In equilibrium, the occupation percentage is given by the Fermi-Dirac function,

$$f = \frac{1}{1+e^{(E_i - E_f)/kT}} \tag{2.8}$$

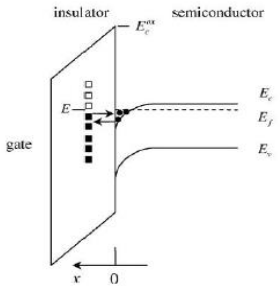

Figure 2.10 Schematic of tunnelling between bulk-oxide traps in the gate insulator and conductance band of the semiconductor [24].

When a slow, incremental gate voltage changes the local potential at x by $\delta\psi$ (x), Et changes by $\delta E_t = -q\delta\psi(x)$, and the trapped charge per volume changes by $\delta Q_t = qN_{bt}(df/dE_t)\,\delta E_t = (q^2/kT)\,N_{bt} f\,(1-f)\,\delta\psi(x)$. Note that δQ_t is proportional to the local potential change, $\delta\psi(x)$, not

the surface potential change $\delta\psi_s$ at $x = 0$. The static effect of the traps is then equivalent to a capacitance (**Figure 2.8**)

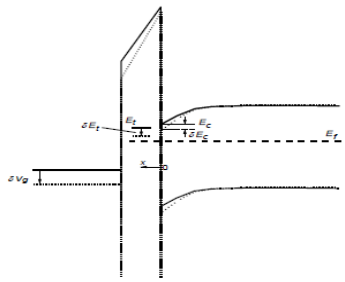

Figure 2.11 Band diagram of MOS capacitor with oxide traps at E and x. The dotted lines show how the bands change with a slight increase of gate voltage [25].

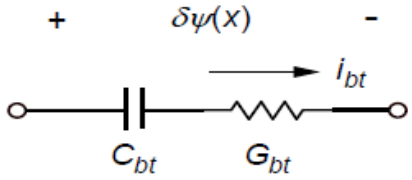

Figure 2.12 Serial circuit representation of a single-level trap element. C_{bt} and G_{bt} are capacitance and conductance per volume.

$$C_{bt} = \frac{q^2}{kT} f(1-\mathrm{f})\,\mathrm{N_t} \tag{2.9}$$

Based on Shockley-Read-Hall theory [26] applied to border traps, the capture rate for traps at x is

$$r_c = c_n n e^{-2\kappa x} N_t (1-\mathrm{f}) \tag{2.10}$$

where n is the conduction band electron density at the semiconductor surface, $e^{-2\kappa x}$ is the attenuation factor from tunneling, and c_n is the capture probability in cm^3/s often expressed as σv_{th} where σ is the trap cross-section area and v_{th} is the electron thermal velocity. κ is the attenuation coefficient for an electron wave function of energy E decaying under an energy barrier $E^{ox}_C > E$

$$\kappa = \sqrt{2m^*(\mathrm{E}_C^{OX} - \mathrm{E})/\hbar} \tag{2.11}$$

m^* is the electron effective mass in the dielectric film and E^{ox}_C is the energy of the top of the dielectric barrier, as indicated in **Figure 2.10**. The emission rate is

$$r_e = e_n N_t f \tag{2.12}$$

where e_n is the emission probability in s^{-1}. In equilibrium, $r_c = r_e$, therefore,

$$\frac{e_n}{c_n n e^{-2\kappa x}} = \frac{1-f}{f} = e^{(\mathrm{E_t}-\mathrm{E_f})/\mathrm{kT}} \tag{2.13}$$

n can be expressed in terms of the conduction band effective density of states N_c as

$$n = N_c \exp[-(\frac{E_C - E_F}{kT})] \tag{2.14}$$

Substituting $c_n = \sigma v_{th}$ and **Equation 2.13** into **Equation 2.12** yields

$$\frac{e_n}{\sigma v_{th} e^{-2\kappa x}} = N_c e^{-(E_c - E_t)/kT} \tag{2.15}$$

The right side is simply the Boltzmann factor for the probability of electron emission from energy E_t to energy E_c. In Appendix I of Nicollian and Brews [1], e_n is treated as a constant because for interface state traps at x = 0, E_c - E_t is fixed. For oxide traps at x, however, $\delta E_t \neq \delta E_c$ (**Figure 2.11**), the change of e_n must be taken into account.

Consider a sudden step V_g that changes the δE_t of oxide traps at x by δE_t and E_c by δE_c. From **Equations 2.13 and 2.14,**

$$\delta n / n = -\delta E_c / kT \tag{2.16}$$

and

$$\delta e_n / e_n = -(\delta E_c - \delta E_t) / kT \tag{2.17}$$

These give rise to instantaneous changes in **Equations 2.15 and 2.17.** Note that the trap occupancy factor f has not changed yet and remains at the value prior to the step. For the case shown in **Figure 2.12**, $\delta E_t < \delta E_c < 0$, the capture rate r_c increases and the emission rate r_e decreases instantaneously. The net charging current is

$$\begin{aligned} i_t &= q(\delta r_c - \delta r_e) = q c_n N_t (1-f) e^{-2\kappa x} \delta n - q N_t f \delta e_n \\ &= q N_t f e_n (\delta n / n - \delta e_n / e_n) = -q N_t f e_n \delta E_t / kT \end{aligned} \tag{2.18}$$

The middle step made use of the relation $r_c = r_e$ before the voltage step. The instantaneous drop of local potential $\delta\psi(x) = -\delta E_t/q$ is entirely over G_{bt} in **Figure 2.14**. So $G_{bt} = i_{bt}/ \delta\psi(x)$ is a simple conductance,

$$G_{bt} = (q^2 / kT) N_t f e_n \tag{2.19}$$

Alternatively, $G_{bt} = \sigma v_{th} n e^{-2\kappa x} (q^2/kT) N_t (1-f)$, and C_{bt} and G_{bt} are related by time constant $\tau(x)$,

$$\tau(x) = C_{bt} / G_{bt} = f \tau_0 e^{2kx} \tag{2.20}$$

which is a function of depth x [27,28]. Here, $\tau_0 = (n_s \sigma v_{th})^{-1}$ is the time constant of the traps at the interface x=0. Note that here a time-domain approach to derive C_{bt} and G_{bt} is used. It is simpler and more physical than the frequency-domain approach in Appendix I of Nicollian and Brews [1] in arriving at the same results.

If the density per volume per energy of bulk-oxide traps is N_{bt} in units of $cm^{-3}Joule^{-1}$, then C_{bt} is re-written to ΔC_{bt} as [26, 27]

$$\Delta C_{bt}(E, x) = \frac{f_0 (1-f_0) q^2 N_{bt}}{kT} \Delta E \Delta x \tag{2.21}$$

and

$$\Delta C_{bt}(\mathrm{E},\mathrm{x})/\Delta \mathrm{G}_{\mathrm{bt}}(\mathrm{E},\mathrm{x}) = \tau(\mathrm{x}) = f_0\tau_0 e^{2\kappa x} \tag{2.22}$$

To integrate for a continuous energy distribution of bulk-oxide traps, the serial connection of $\Delta C_{\mathrm{bt}}(E, x)$ and $\Delta G_{\mathrm{bt}}(E, x)$ at a given x must be first converted to a parallel combination of incremental admittance. Because the factor $f_0(1 - f_0)$ is sharply peaked at $E = E_f$, κ in **Equations 2.16** is set to be a constant with $E = E_f$ in the integration. The total incremental admittance at x is then

$$\Delta Y_{bt}(\mathrm{x}) = \int_E \frac{1}{\dfrac{1}{j\omega\Delta C_{bt}(\mathrm{E},\mathrm{x})} + \dfrac{1}{\Delta G_{bt}(\mathrm{E},\mathrm{x})}} = \frac{q^2 N_{bt}\ln(1+\mathrm{j}\omega\tau_0\,\mathrm{e}^{2\kappa\mathrm{x}})}{\tau_0 e^{2\kappa x}}\Delta x \tag{2.23}$$

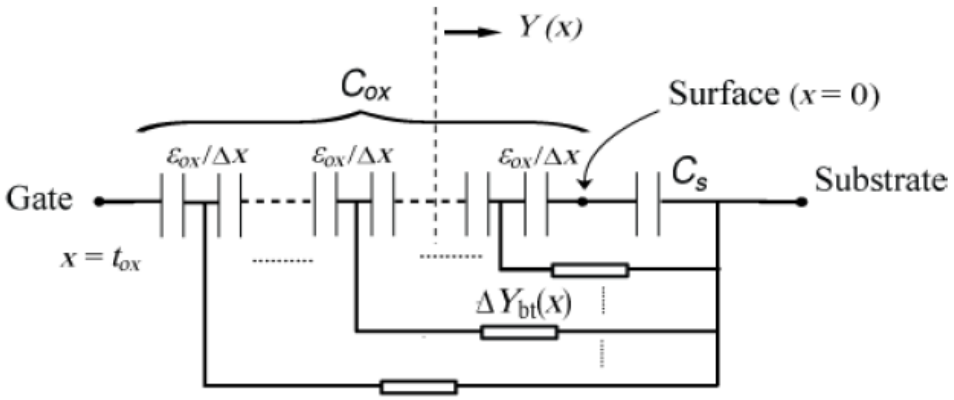

Figure 2.13 Equivalent circuit for bulk-oxide traps distributed over the depth of the insulator [25].

If we define $Y(x)$ to be the equivalent admittance at a point x looking into the semiconductor in **Figure 2.14**, the recursive nature of the distributed circuit gives the admittance of the next point $x+\Delta x$ as

$$Y(\mathrm{x}+\Delta\mathrm{x}) = \Delta\,\mathrm{Y}_{\mathrm{bt}} + \frac{1}{\dfrac{\Delta x}{jw\varepsilon_{ox}} + \dfrac{1}{Y(\mathrm{x})}} \tag{2.24}$$

Substituting **Equation 2.24** for $\Delta Y_{bt}(\mathrm{x})$, the first-order terms in Δx then yield a differential equation for $Y(\mathrm{x})$

$$\frac{dY}{dx} = \frac{-Y^2}{jw\varepsilon_{ox}} + \frac{q^2 N_{bt}\ln(1+\mathrm{j}\omega\tau_0\,\mathrm{e}^{2\kappa\mathrm{x}})}{\tau_0\,\mathrm{e}^{2\kappa\mathrm{x}}} \tag{2.25}$$

The boundary condition is $\mathrm{Y}(\mathrm{x}=0) = \mathrm{j}\omega\mathrm{C_s}$. **Equation 2.25** is numerically solved to obtain the total admittance seen by the gate:

$$Y(\mathrm{x}=\mathrm{t_{ox}}) \equiv \mathrm{G_{tot}} + \mathrm{j}\omega\mathrm{C_{tot}} \tag{2.26}$$

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Chapter 3: A brief Study on the Effects of Post-Deposition Annealing for ALD-Deposited Al_2O_3 on an n-Type Silicon Substrate

3.1 Introduction

A large band gap and an exalted barrier height between the dielectric and Si has essential chemical, along with the thermal steadiness of the conventional dielectric material silicon dioxide (SiO_2), on silicon (Si) wafers [1–3]. However, the applicable SiO_2 layer thickness (which functions as the insulating layer) reaches its maximum owing to the miniaturization of metal–oxide–semiconductor field-effect transistors (MOSFETs). Because of direct tunneling through the SiO_2 film, low-power application devices mostly agonize from high leakage currents [4]. Nevertheless, the leakage current and equivalent oxide thickness (EOT), which are associated with the speed of the transistor, can be decreased with a denser oxide layer with a high dielectric constant (k). Among the different deposition techniques, such as physical vapor deposition, chemical vapor deposition (CVD), and atomic layer deposition (ALD) for high-k oxides, ALD [5–9] is considered the most promising technique for studying the microelectronic and nanotechnological characteristics of samples. Being a subtype of CVD, in ALD, at the same time in the deposition chamber, the precursors and oxidants are not only present but also introduced in a chronological and noncongruent way. The continuous purge gas flow eradicates residual precursors and reactant species between the precursor and oxidant inoculations. The combination of the precursor/oxidant pulses and purge gas flow is acknowledged as a half cycle; the film is deposited through this self-saturating half cycle because the reactions stop once all reactive components on the Si surface are devoured. Throughout this process, the reactions are eradicated by themselves [9]. Therefore, deposition occurs in a cyclic order in ALD, whereas it happens on a time basis in CVD [5]. The thickness of the deposited film can be accustomed to the number of deposition cycles. Thus, the self-saturating nature and cyclic deposition deliver amenable, disciplined, uniform, high-quality, condensed, and pinhole-free thin films with thickness errors of less than 1%; the film growth is autonomous of the precursor and oxidant flux [7,10]. The different deposition procedures (including ALD) are comprehensively compared in [9]. Al_2O_3, which is one of the studied high-k oxides, is considered to be one of the most auspicious substitutions for SiO_2 because of its simple ALD manufacturing process [11]. Al_2O_3 has a higher bandgap (approximately 8.8 eV) and band orientation analogous to SiO_2, good thermal steadiness, and concentrated oxygen and ionic carriage, with a reasonable dielectric constant (k = 6–9) [12,13].

Post-metal annealing (PMA) and post-deposition annealing (PDA) are two methods of rapid thermal annealing (RTA) used to observe the features of MOSCAPs. This observation can be conducted at different temperatures for different durations in an ambient gas environment. For the Al_2O_3 MOSCAP, numerous research studies have been conducted on PMA characteristics [14–16]. In PMA, after the fabrication of the oxide layer and metal layer on the semiconductor, the MOSCAP is annealed at a specific temperature for a definite time in a suitable ambient gas condition. In PDA, the MOSCAP is annealed after the fabrication of the oxide layer and before the deposition of the metal layer. Researchers have discovered that a slowly increasing PMA temperature makes the capacitance value reduced and the leakage current enlarged. These outcomes signpost that PMA with aluminum electrodes is substantially subtle to the annealing condition compared with PDA [17]. Additionally, PMA ought to have higher value of equivalent oxide thickness (EOT) and interface state density as compared with

PDA. Besides, there is no frequency dependence in the case of PDA found in the weak inversion region of capacitance–voltage (C–V) curves of PMA annealed samples [17]. According to [18,19], PDA can affect the capacitance, hysteresis, dielectric constant, and morphological structure, but constant voltage stress, interface, and border trap characterizations are not clearly stated in those articles. The shift in the threshold voltage after constant voltage stress should generally differ from MOSCAP to MOSCAP based on the annealing conditions (e.g., duration, temperature, and ambient gas environment). In this paper, all these attributes, along with the constant voltage stress for the $Al/Al_2O_3/n$-Si MOSCAP regarding PDA, are discussed.

The flat-band voltage, V_{FB} (which is the gate voltage at which the energy bands in the semiconductor substrate remain horizontal with respect to the semiconductor–dielectric interface and at which the surface potential of the semiconductor substrate is zero), is one of the most critical parameters of a metal–oxide–semiconductor (MOS) structure. The importance of this parameter is attributable to the fact that it is a critical feature of the threshold voltage, VT, of the MOS transistor and its diverse uses for other characteristics of MOS structures [20]. The shift of the flat-band voltage in the positive direction in the C–V curve is a prominent problem of Al_2O_3 films. The positive shift is due to negative charge traps in the oxide layer induced by Al diffusion from the Al_2O_3 layer to the Si substrate [21,22]. When the annealing temperature increases, the diffusion rate increases. In addition, because neither optical nor electrical impulses are applied, free charges must be created by the trapping or detrapping defects inside the dielectric; the energy required to trigger this mechanism can only be provided by temperature (i.e., phonons). The bulky shift of the flat-band voltage upsurges the Coulomb scattering between carriers and trap charges. This causes the catastrophic reduction of the conductance of the carrier. Researchers have stated that the variations in the chemical states and atomic structures of films are strongly linked to these phenomena [21–24]. Because Al3+ diffuses into the Si substrate, the density of positive ions (holes) in the semiconductor increases, which attracts more negative charges (electrons). Thus, n-type Si, which usually functions as the donor, starts to function as the acceptor. Moreover, as the atomic radius of Al (143 pm) is larger than that of Si (118 pm) [25], diffusion is accompanied by some scattering events in usual Si atomic structures. These phenomena may change the attributes of samples that have been annealed at high temperature and are subjected to constant voltage stress. Constant voltage stress measurements are conducted to determine how a MOSCAP device reacts when a gate bias is applied for a specific duration; in these measurements, unusual properties such as strain instead of stress can occur after certain PDA conditions. In this study, some other hallmarks of MOSCAP characterization, such as interface trap density (D_{it}) and border trap (N_{bt}), are extracted. To determine the D_{it} of dielectric/semiconductor (SiO_2/Si) interfaces of MOSCAP structures, researchers developed different approaches in the 1960s [26]. High interface trap densities are the reason for unproductive Fermi level response. In addition, they can cause Fermi level pinning, thereby preventing the successful control of charge carriers in the channel and the comprehension of MOSFETs with good subthreshold slopes and high drive currents, although Si possesses high-quality native oxides with good stability, low leakage, and high breakdown fields. To extract the D_{it}, the conductance method was used in this study, as recommended in [26]. Owing to the time constant difference between both forms of traps and the border trap density estimate from the C–V hysteresis, which exhibits full re-emission of captured charges during the reverse C–V sweep, the traditional interface trap model does not explain the existence of border trap phenomena. Their existence must be proved based on the

dispersion of accumulated frequencies [13,27]. Many researchers have investigated border trap reduction caused by annealing; nevertheless, the annealing environment and its effects have not been studied thoroughly [28,29]. A robust method for border trap extraction is presented in [29–32]; the same strategy was used in this study.

3.2 Materials and Methods

The Al_2O_3 thin film was deposited with a thermal ALD system. The deposition temperature was 250 °C, and an n-type Si (100) substrate (Sehyoung Wafer Co. Ltd., Seoul, Korea) with 1–100 W cm resistivity and try-methyl aluminum (TMA) as the precursor for Al_2O_3 were used. The Chemical Abstracts Service number of TMA is 75-24-1; it has 99.99% purity according to UP Chemical Co., Ltd. (Pyeongtaek, Korea). H_2O was used as the oxidizing agent, and argon was the carrier and purge gas. The ALD system consisting of an allocation system with four sets of precursor canisters conducted the thermal ALD process ("Atomic Classic", CN1, Hwaseong, Korea) at a maximal deposition temperature of 450 °C. The TMA precursor was kept at room temperature. The carrier and purge gas flow rates for Al_2O_3 deposition were 0.3 L/min. Moreover, the pulse time was 0.1 s, and the purge time was 20 s. The oxidant (H_2O) pulse and purge times were 0.1 s and 60 s, respectively. The Al_2O_3 layer was deposited with 100 cycles. Before deposition, the substrate was processed with a standard precleaning method with acetone, isopropyl alcohol, and deionized water. Subsequently, the substrate was dried in a N_2 environment for the prevention of watermark formation on the surface. Eight samples were prepared for oxide layer deposition. The deposition started with pre-argon purging, 100 cycles of Al_2O_3 deposition as the second step, and post-argon purging as the third step. The thicknesses of the ALD-deposited films were measured with ellipsometry at an incident angle of 70°. Because all eight samples had been simultaneously covered with Al_2O_3, their oxide thicknesses were approximately identical. The average calculated growth per cycle (GPC) was 1.14 Å. For the PDA process of the substrates, the Nextron TM rapid thermal processing system RTP-1200 and Atovac flow and pressure controller GMC1200 were used. The RTA time and temperature were as follows: 300 °C–2 min, 300 °C–5 min, 300 °C–10 min, 400 °C–2 min, 400 °C–5 min, 500 °C–2 min, and 500 °C–5 min; the resulting characteristics were compared with those of as-grown substrates that were not treated with PDA. Instead, they were pre-annealed at 100 °C for 1 min. To prepare MOSCAP devices, an approximately 150 nm thick Al metal layer was deposited with a thermal evaporator (Korean vacuum thermal evaporator system, KVT-438) on the dielectric to create front electrodes with different areas with a shadow mask: 200, 300, and 400 μm^2. The same metal layers were deposited without masks as back contacts. The electrical characterization (e.g., the C–V and constant voltage stress measurements) and interface and border trap extractions were performed with a probe station (MSTech 5500), semiconductor device analyzer (Keysight B1500A), waveform generator/fast measurement unit (Keysight B1530A), precision LCR meter (Agilent 4284A), and low-leakage switch mainframe (HP E5250AX-Ray diffraction (XRD) was measured by an X-ray diffractometer (Rigaku Ultima 4) where, Cu Kα radiation (40 kV, $\lambda = 1.54$ Å) was used for measuring. Various conditions for preparing the MOSCAPs are shown in Table 3.1.

Table 3.1 Conditions of parameters used for MOSCAP fabrication.

		ALD			RTA		Thermal Evaporator
Sample	**Oxide**	**Cycle**	**Temperature**	**Gas**	**Temperature**	**Time (min)**	**Metal Layer**
As-Grown	Al_2O_3	100	250	Ar	-	-	Al
300 °C–2 min		100	250	Ar	300 °C	2	
300 °C–5 min		100	250	Ar	300 °C	5	
300 °C–10 min		100	250	Ar	300 °C	10	
400 °C–2 min		100	250	Ar	400 °C	2	
400 °C–5 min		100	250	Ar	400 °C	5	
500 °C–2 min		100	250	Ar	500 °C	2	
500 °C–5 min		100	250	Ar	500 °C	5	

3.3 Results & Discussion

Figure 3.1 demonstrates the C–V characteristics of the Al_2O_3 MOS capacitors (PDA) annealed at different temperatures for different times at 1 MHz. The colored curves represent the capacitance values of the MOSCAPs. The MOSCAP annealed at 300 °C for 5 min has the highest capacitance, and the 500 °C–5 min sample has the lowest; the As Grown and other samples have similar values except sample 400 °C–5 min; its capacitance value is lower than that of 300 °C–5 min and higher than those of the others. The C–V curves of the samples are fluctuating towards right side as PDA time and temperature extend. The curves of the as-grown to 400 °C–5 min samples are close; however, those of the samples annealed at 500 °C shift abundantly. When a C-V curve is shifting towards positive side, that means the threshold voltage as well as flat band voltage (V_{FB}) is also increasing.

Figure 3.2a shows the V_{FB} value of each sample; it gradually increases with increasing PDA time and temperature. The V_{FB} values of the samples were calculated with the inflection point method using a second derivative of the C-V curve. The point of intersection of second derivative of the CV curve with the Vg-axis is zero, which is called the inflection point as well as the value of flat band voltage[1]. Most researchers have stated that V_{FB} shifts owing to ion diffusion at the annealing temperature[2–5]; this results in an additional aluminum silicate layer at the interface of the Si substrate and oxide layer, as presented by the X-ray diffraction (XRD) data in Figure 3.2b (each sample exhibits peaks at 82.5°)[34]. For the XRD measurements, the annealing time was set to 5 min and the temperature was 300, 400, and 500 °C. We measured 2θ from 30˚ to 90˚, but significant difference in the peak analysis, in terms of annealing, is not found except in 2θ=82.5 ˚. From the literature[6–8], we found, this value of 2θ, indicates the presence of aluminium silicate. That is why, we have narrated down the whole XRD waveform into around 80 degree. The peak variations among the four samples indicate that the increasing temperature promotes diffusion in the interfacial layer. The peak of the sample annealed at 500

°C is much higher than those of the others; this confirms greater diffusion at 500 °C. In the n-Si samples, the shift of V_{FB} to the right means that Al^{3+} ions from the Al_2O_3 layer diffuse toward the Si substrate.

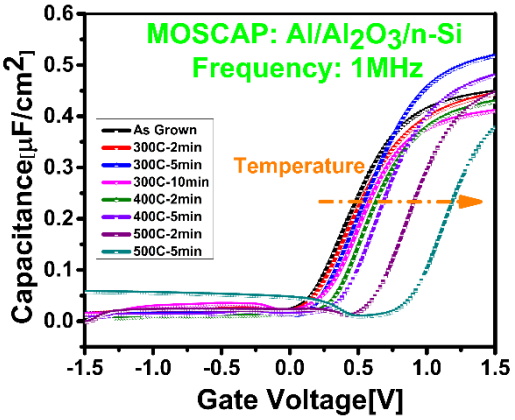

Figure 3.1. Capacitance-Voltage Curves Comparison at 1 MHz.

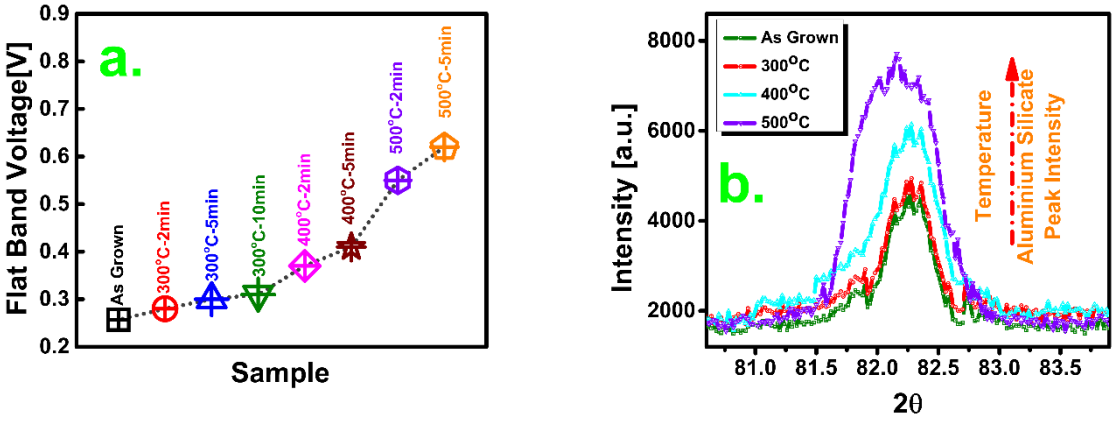

Figure 3.2. (a) Flat Band Voltage Comparison by Inflection Point Method; (b) XRD peak value indicating Aluminium Silicate presence.

Figure 3.3a compares the dielectric constants of the samples. The 300 °C–5 min sample has the highest dielectric constant because the constant depends on the capacitance value. The dielectric constant is calculated as follows [9]:

$$\varepsilon_{high-k} = \frac{C_{max} \times T_{ox}}{\varepsilon_0} \quad (1)$$

Figure 3.3b presents the hysteresis results. Accordingly, the 300 °C–5 min sample has the lowest hysteresis. In general, the Al_2O_3 hysteresis is inversely proportional to the PDA time and temperature. However, above certain temperature and time thresholds, the hysteresis increases; this increase is still lower than that of the as-grown sample (which has no PDA-annealed MOSCAP). Highest capacitance and hysteresis were measured in several devices in each of the MOSCAP to make sure about the trend. All test and average calculation results as well as the calculated standard deviation of the seven samples are listed in Tables 3.2 and 3.3. The standard deviation indicates how disperse the data is in relation to the average value. For

example, in Table 2, the standard deviation values indicate that, 300°C_5min sample has the lowest scattering in terms of hysteresis.

Table 3.2. Highest capacitance values of tested devices

	As Grown	**300 °C 2 min**	**300 °C 5 min**	**300 °C 10 min**	**400 °C 2 min**	**400 °C 5 min**	**500 °C 2 min**	**500 °C 5 min**
Test 1	0.46	0.47	0.54	0.43	0.42	0.47	0.45	0.48
Test 2	0.38	0.52	0.53	0.45	0.45	0.47	0.53	0.52
Test 3	0.375	0.34	0.53	0.43	0.42	0.51	0.52	0.46
Test 4	0.48	0.46	0.53	0.38	0.51	0.50	0.43	0.29
Test 5	0.475	0.4	0.53	0.46	0.43	0.46	0.54	0.52
Test 6	0.375	0.35	0.56	0.40	0.44	0.44	0.48	0.27
Test 7	0.45	0.45	0.475	0.48	0.50	0.52	0.475	0.425
Avg	0.43	0.43	0.53	0.43	0.45	0.48	0.49	0.42
STD	0.05	0.07	0.03	0.03	0.04	0.03	0.04	0.1

Table 3.3. Hysteresis data of tested device

	As Grown	**300 °C 2 min**	**300 °C 5 min**	**300 °C 10 min**	**400 °C 2 min**	**400 °C 5 min**	**500 °C 2 min**	**500 °C 5 min**
Test 1	30.0	13.6	10.9	17.6	42.0	33.4	9.0	13.2
Test 2	55.5	31.3	2.2	40.7	56.6	58.2	14.6	22.2
Test 3	55.6	36.8	8.2	34.1	32.1	36.5	26.5	76.2
Test 4	53.7	6.1	2.4	54.3	28.1	28.7	2.5	9.4
Test 5	52.6	62.9	1.9	65.0	23.5	27.0	33.7	15.7
Test 6	51.1	36.8	0.4	33.5	49.0	44.5	3.9	10.4
Test 7	34.3	70.7	10.4	27.2	34.0	22.3	24.1	61.8
Avg	47.5	36.9	5.2	38.6	37.9	35.8	16.3	29.8
STD	10.7	23.6	4.5	16.1	11.8	12.2	12.0	27.4

Figure 3.4a exemplified the interface trap density (D_{it}) of the samples and as-grown sample under different treatment conditions; the trap density was calculated with the conductance method by considering the series resistance correction with the following equation:

$$D_{it} = \frac{2.5}{Aq} \times \left(\frac{G_p}{\omega} \right)_{max} \quad (2)$$

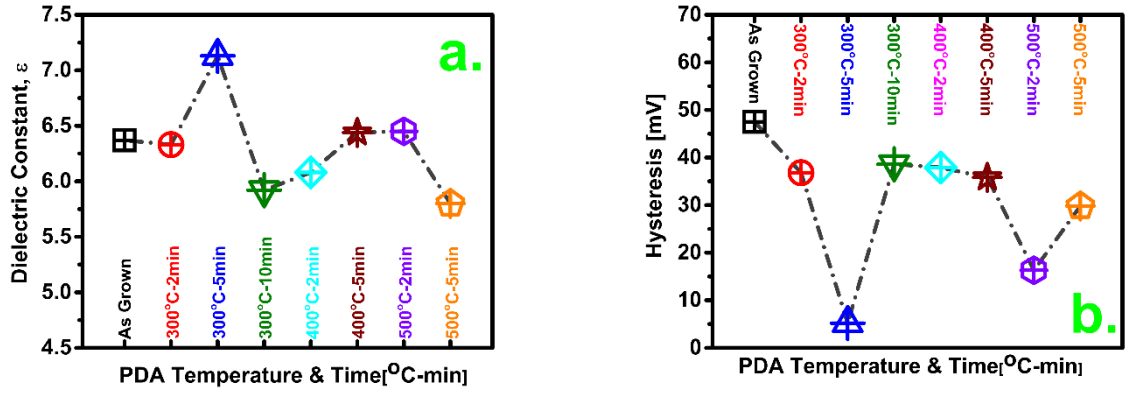

Figure 3.3. (a) Average dielectric constants; (b) comparison of average hysteresis.

where, A is the area of the measured device, q the electron charge, G_p the parallel conductance, and ω the angular frequency. [9] The D_{it} values of the As Grown, 300 °C–2 min, 300 °C–5 min, 300 °C–10 min, 400 °C–2 min, 400 °C–5 min, 500 °C–2 min, and 500 °C–5 min samples are $5.8*10^{11}$, $5.6*10^{11}$, $4.94*10^{11}$, $1.32*10^{11}$, $5.06*10^{11}$, $5.1*10^{11}$, $3.7*10^{11}$, and $2.67*10^{11}$ $cm^{-2}eV^{-1}$ because all samples had identical interfaces and Al_2O_3 layer thicknesses and the same pre-treatment. The D_{it} pattern exhibits two characteristics. First, the increasing annealing time decreases D_{it} (the 5 min time frame presents a greater reduction in the density of interface traps than the 2 min case). Second, the interface trap density decreases more at 500 °C than at 300 °C, although there is a little discrepancy in the 400 °C cases. Thus, a high annealing temperature and long annealing time effectively reduce D_{it}.

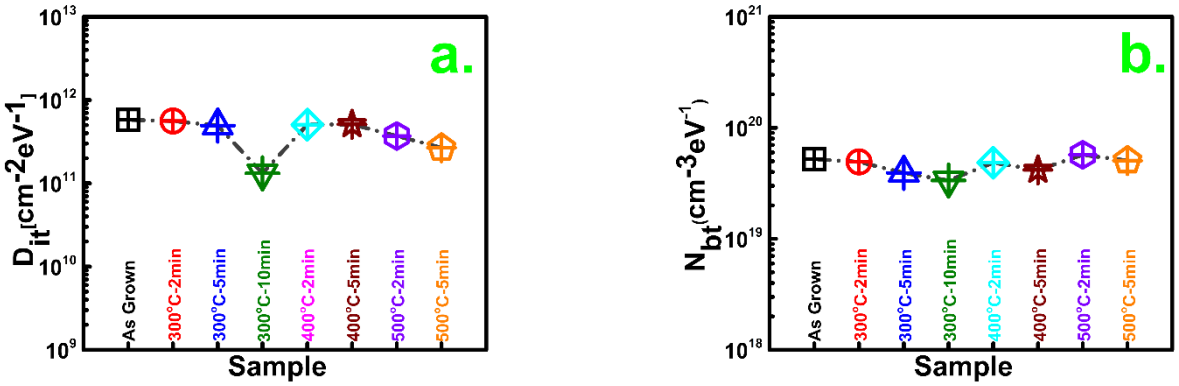

Figure 3.4. (a) Interface Trap Comparison; (b) Border Trap Comparison; for all samples.

Figure 3.4b presents the extracted border trap densities, N_{bt}, of the MOSCAPs. They were determined with the distributed border trap model proposed by Yaun et al. by constructing the best fit between the measured capacitance at the precise voltage in the accumulation region and the capacitance calculated from the model [10]. The overall oxide thickness is segmented into a limited number of quantities in this model. Each quantity reflects a certain oxide capacitance that is proportional to the border trap extent and arranged in series with the semiconductor capacitance in a parallel admittance model. In [11,12], the Nbt model and extraction method

were thoroughly described. In the extraction process, the effective electron mass of the Al_2O_3 film was considered $0.23m_0$, where m_0 represents the electron rest mass [13,14]; the trap capture/emission time constant $\tau 0$ was a fitting parameter. In addition, a one-dimensional Poisson–Schrodinger solver simulation tool (next Nano) was used to calculate the semiconductor capacitance C_s at the border trap extraction voltage [15]. Here, almost same pattern was observed as interface trap density (D_{it}) in the extracted densities of border trap. Many of these special oxide traps disappear at high annealing temperature and with longer annealing time, which is supposed to more stoichiometric change at these conditions. According to figure 3.4(b), the 300 °C–10 min MOSCAP has the lowest amount of border traps.

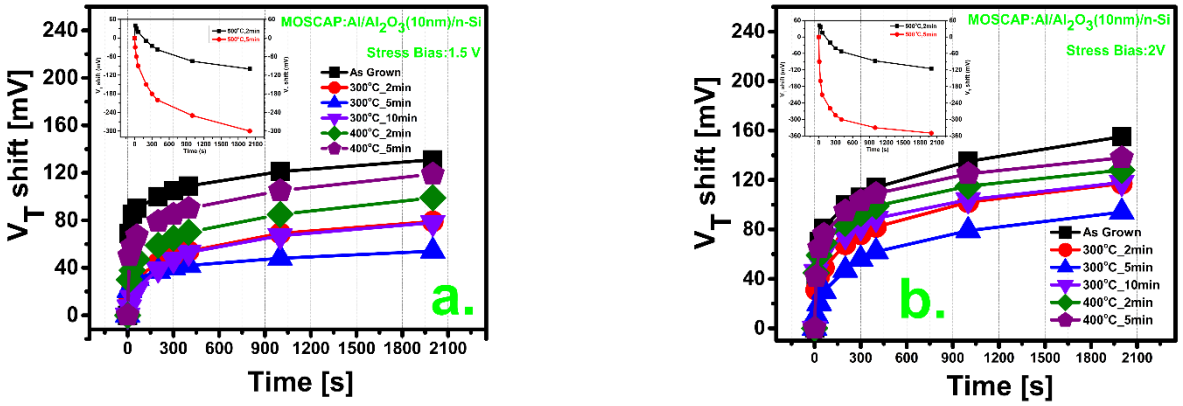

Figure 3.5. Threshold voltage shift after application of constant voltage stress for 2000 s: (a) 1.5 V stress bias, (b) 2.0 V stress bias. Inset: 500 °C samples after stress application.

Figure 3.5 shows the V_T shifts in the constant-voltage stress measurement. The CVS was measured at 1.5 and 2.0 V stress bias for 0, 10, 30, 60, 200, 300, 400, 1000, and 2000 s. The V_T shift indicates how much degradation occurred due to stress in the sample. Figures 5a and b both designate that 300°C-5min annealed sample has the lowest dispersion after stress for both stress bias voltages, while the As Grown sample has the highest dispersion and other MOSCAPs are in the intermediate range. Evidently, the post deposition heat treatment improves the film quality. However, at relatively high temperature, the scenario has dramatically changed. According to the insets in Figures 5a and b, in the results of samples 500 °C–2 min and 500 °C–5 min, the V_T shifts left after the stress treatments. This is probably due to excessive ion diffusion from the oxide layer to the n-Si substrate. Because positive Al^{3+} ions diffuse to the Si layer, the electron concentration of the n-doped Si layer may be changed[5]. The increase in positive ions (holes) reduces the number of negative ions (electrons). Consequently, the n-Si layer, which has functioned as the donor, attracts more electrons and, therefore, functions as the acceptor. Constant-voltage stress experiments on MOSCAPS have not been performed; according to the results, this is the most convenient and realistic explanation for this behavior. Therefore, there is a possibility of some changes in lifetime of the MOS capacitors in terms of annealing [16]. The relation between lifetime and annealing conditions will be further discussed in an extension of this work.

Figure 3.6 presents the leakage current densities and breakdown voltage characteristics transformation in various PDA condition after applying a positive bias voltage from 0 to 15 V. Sample 300 °C–5 min exhibits the lowest leakage current and highest breakdown voltage among all the samples; with increasing PDA time and temperature, the MOSCAP breaks down

at a lower voltage. As a result, sample 500 °C–5 min has the lowest breakdown voltage and highest leakage current. This behavior can be described with ion diffusion theory. Because the surface morphology has changed with increasing temperature, the interface between the oxide and semiconductor becomes leakier and cannot absorb the high bias voltage.

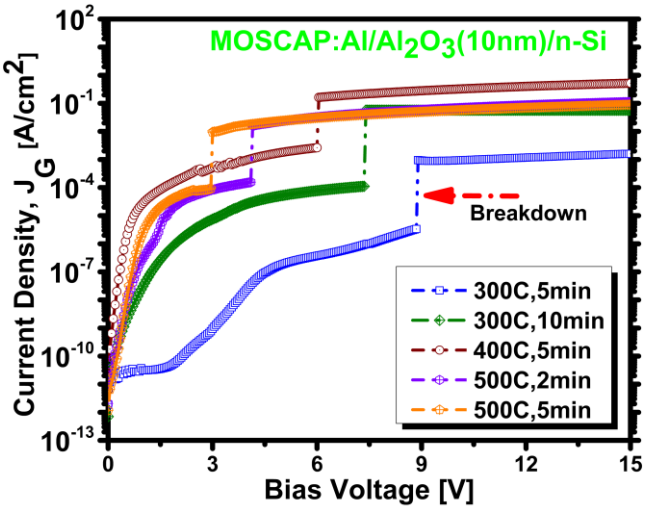

Figure 3.6. Breakdown voltage and leakage current of MOSCAPs.

3.4 Conclusions

In this study, the characteristics of Al_2O_3 PDA-annealed under different conditions on Si substrate were investigated. The Al_2O_3 layers were deposited with H_2O as an oxidant and ALD. The capacitance, hysteresis, dielectric constant, constant voltage stress, leakage current, breakdown voltage, interface trap, and border trap characteristics of annealed and non-annealed samples were compared. In addition, their surface morphologies were studied with XRD. The results clearly indicate that the annealed samples show better characteristics than the non-annealed samples. Moreover, the diffusion properties of the silicon and oxide layers were discussed. This article divulges an unopened scenario and also presents the optimal conditions for post deposition annealing of Al/Al_2O_3/n-Si stacks.

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Chapter 4: Optimization of atomic layer deposited high-k oxides for AlGaN/GaN MOSHEMT.

4.1 Introduction

For many years, the reduction in size of the semiconductor device was believed to be the driving factor behind the success of High Electron Mobility Transistor for frequency and high-power switching applications [1]. A continues decrease in the dimension of transistor has improved the device electron densities which led to the extraordinary improvement in high power switching application and frequency performance which also led to reduction of the cost of the power devices as well. Technically, scaling of the transistor's size has come to an end because the silicon CMOS (Complementary Metal Oxide Semiconductor) Field Effect Transistor (FET) have reached their fundamental physical limit [2], due to current leakage under the device's gate and saturation of the supply voltage. This however, causes device's high consumption of power which has been the largest problem of advanced (CMOS) technology today [3].

GaN based High Electron Mobility Transistor (HEMTs) have attracted the attention of many researchers due to its superior material surface properties than its contemporary Silicon (HEMTs). Under high temperature and high voltage, GaN (HEMTs) exhibits extraordinary performance in frequency and power switching application, making it more favourable alternative to replace the existing Silicon Complementary Metal Oxide Field Effect Transistor [4]. However, GaN is a wide bandgap material having a bandgap of about 3.4 V which allow the transistor to operate under high temperature and remain fully functional at the temperature of 300 °C and above and maintaining excellent control of the current in the channel [5]. Nevertheless, the main obstacle which prevents GaN HEMT from widespread use is its normally-on behavior, since the two-dimensional-gas buried in between the AlGaN/GaN interface remains a high density to neutralize the strong polarizations between this heterointerface. In common power converters, switches are required to remain normally-off when gate drivers output zero voltage, but a negative turn-off gate voltage for GaN HEMTs demands high gate driver complexity and increases the risk of circuit failure [6].

Self-heating needs to be incorporated into the models of the devices. [7] Self-heating can be clearly seen in the dc characteristics, but determination of the actual temperature increases in the devices themselves is not easy, especially in the active channel. Useful methods to observe the temperature distribution around a device include liquid crystal thermography [10] and micro-Raman spectroscopy. [8] The latter probes the average temperature of the GaN, not just the channel temperature. The average temperature increase is influenced by the device layout, as well as the choice of substrate and other materials involved in conducting the heat away. This work builds on the approach of only using electrical device measurements to estimate the self-heating [9].

Highly efficient GaN-based high electron mobility transistors (HEMTs) for power applications require an insulated gate structure in order to suppress parasitic gate leakage currents. In such MIS-HEMTs, in contrast to Schottky devices, a drift of the threshold voltage under forward gate bias is an often observed but rarely investigated phenomenon and usually related to trapping at the dielectric/III-N interface [10]. Previous investigations of this interface based on

photo assisted CV-measurements, admittance measurements or DTLS-like measurements [11] are mainly focusing on determining the interface trap density [12]. The performance and precise Vth adjustment of GaN MOS-HEMTs is still limited by the presence of traps related to the gate oxide, partly also due to a lack of effective characterization techniques. In fact, very few capacitance techniques for interface trap density (D_{it}) determination in GaN MOS-HEMTs have been adopted so far. This is because of several interfaces present in the GaN MOS-HEMT structure and a wide band gap nature of GaN, making conventional techniques (known from Si MOS technology) for D_{it} determination inapplicable. Moreover, these techniques usually neglect other parasitic effects such as trapping in the bulk oxide traps, often present in GaN MOS-HEMTs.

Researchers have proposed several methods for modelling the dispersion of capacitance at accumulation and making electrical characterizations of border traps [10,17–23]. Among them, the distributed border trap model from Yuan et al. is the most well-known [10,23]. In this model, the oxide thickness (t_{ox}) is segregated into immeasurable quantities of small fragments, with each part contributing an amount of oxide capacitance, ΔC_{ox}, connected in parallel with the admittance proportional to the border trap density; this parallel combination is connected in series with the semiconductor capacitance. The border trap density is then extracted by making a best-fit condition between the calculated capacitance and the conductance achieved from this model and experimental values. Usually, this oxide thickness is mainly the physical thickness (t_{ox}) or EOT, which is the result of either ellipsometry or transmission electron microscopy analysis. While determining the semiconductor capacitance Cs, it is not clear that previous studies' consideration about the quantum mechanical effect [17]. For practical purposes, this capacitance is not only the oxide capacitance but also a series combination of inversion capacitance (C_{inv}), which includes quantum capacitance (C_Q) and centroid capacitance (C_{cent}), by assuming that the first electron sub-band in the channel is occupied [24],[25]. Therefore, the total capacitance includes a series combination of insulator capacitance (C_{ins}), quantum capacitance (C_Q), and centroid capacitance (C_{cent}). In a large-scale device, the series combination of C_Q and C_{cent} is larger than C_{ox}, so the gate capacitance approaches only C_{ox}. However, in small-scale devices, the oxide thickness is on a nanometer scale; thus, C_{ox} becomes commensurate with the other components of total capacitance[24].

Quantum capacitance (C_Q), which is proportional to the DOS of the channel material, physically originates from the Fermi-level penetration onto the conduction band. In the III–V channel material, a two-dimensional electron gas requires energy to be created in the semiconductor quantum well region because of low density-of-states (DOS). Therefore, the Fermi level moves above the conduction band to increase the charge in the quantum well. This movement requires energy and conceptually is equivalent to quantum capacitance. However, charges in the quantum well take a bell-shaped distribution rather than distributing themselves in a sheet form with zero thickness, which means that the physical distance of each charge is quite different from the metal gate. Moreover, the center of the charge distribution may be away from the insulator–semiconductor interface due to the confinement in the quantum well. These effects should be considered when modelling the total capacitance. When these factors are excluded, the overall capacitance is overestimated, so the extracted border trap density (N_{bt}) is inaccurate[26]. To improve the extraction of border trap density, total semiconductor capacitance (C_s) should be included with the quantum confinement effect and band nonparabolicity in the model. Additionally, because of the quantum mechanical confinement

consequence of the carriers, the supplementary thickness of the conductive channel should be considered because the charge centroid in the conductive channel is located deeper beneath the interface of the dielectric and semiconductor, as described previously[27]. Capacitance-equivalent thickness (CET) reflects a more realistic set-up because it considers the above-mentioned effect. Therefore, border trap extraction using a CET metric is a more reliable way to obtain the accurate density of border traps. In this study, we used the CET metric for the extraction of N_{bt} in addition to using physical thickness. In addition, because a border trap is an oxide's native property, the parameters of oxide growth from atomic layer deposition (ALD) must have some effects on border trap formation. In this regard, we also examined the effects of ALD growth temperature on border traps. Moreover, several studies have passivated border traps using a variety of annealing processes[14,28]. Thus, we also examined the passivating effects of two types of annealing processes on border traps. Lastly, the interface trap density (D_{it}) was also extracted for samples that were differentiated with the passivation scheme [18].

Laminated layers may find applications in several fields and in the case of microelectronics devices they have been considered as dielectric insulators, for integration with semiconducting materials such as Si, SiC, GaAs and GaN. In this context, the impressive development of complementary metal-oxide-semiconductor (C-MOS) technology has been mostly associated with the important properties of the SiO_2–Si system. Silicon oxide, the first dielectric material used in the MOS structures, still possesses numerous advantages due to the very low interface defect density, as expected for native oxides, to the high melting point (1713 °C), to the wide band gap (9 eV), to the high resistivity and finally to the good dielectric function (10^7 V/cm). The main drawback is associated with the rather low dielectric constant ε_R = 3.9, which precludes any further decrease of silicon-based device size and with the occurrence of a not ideal interface on wide band gap semiconductors SiC, GaAs and GaN. Problems associated with the choice of the gate insulator, can be solved by adopting alternative layers of new dielectric materials having higher dielectric constant values [29]. Thus, all the materials possessing dielectric constant values higher than ε_{SiO2} = 3.9 are defined "high-k dielectrics". The use of alternative high-k materials favors downsizing of the device while keeping constant their capacitance values and reducing the leakage current density. In this context, huge efforts are nowadays devoted to the fabrication of multicomponent systems having high dielectric constants and good chemical stability. In particular, the growth of Al_2O_3–HfO_2 laminated layers is among the most used combination not only for silicon-based microelectronics devices but also in power electronics devices based on wide band gap semiconductors substrates such as gallium nitride and silicon carbide [20,21] substrates. The choice of the Al_2O_3–HfO_2 system is motivated by the possibility to combine the complimentary characteristics of the two materials. In fact, Al_2O_3 attracted great interest because of its excellent chemical and thermal stability, large band gap (around 9 eV), and large band off-set with different semiconductor substrates (Si, GaN, SiC). Its disadvantageous parameters, on the other hand, are the relatively low dielectric constant (about 9) and the high oxide trap charge density. In the case of HfO2 dielectric oxide, great attention has been devoted to the high dielectric constant (about 25), low leakage current and high reliability although the structural transition from amorphous to monoclinic crystalline phase occurs at low temperature (about 500 °C) and its bandgap is relatively small (5.5 eV) [20]. Therefore, nano laminated structure composed of the two high-k oxides is a promising solution for enhancing thermal stability and sustaining a high dielectric constant value [29].

4.2 MOSCAP Processing and extraction of EOT and CET

Equivalent Oxide Thickness (EOT), represented by t_{eq}, is the gate oxide thickness of the SiO_2 layer of a transistor that would be required to achieve similar capacitance density as the high-k material used. A gate dielectric with a dielectric constant that is substantially higher than that of SiO_2 will initially have a much smaller equivalent electrical thickness. This key feature allowed for the industry to continue on with Moore's Law. As the semiconductor industry began to experiment with transitioning from a SiO_2 gate oxide to a high-k material, EOT can be used to quickly compare those materials using existing SiO_2-based models. In conventional Si-based MOS devices, values of quantum capacitance (C_q) and centroid capacitance are comparatively large, so the total gate capacitance approaches the oxide capacitance (C_{ox}). However, in small scaled III-V based MOS devices these capacitances tend to be smaller and comparable to oxide capacitance (C_{ox}) and lead to a smaller total gate capacitance (C_g). In determining the oxide thickness, generally physical thickness (t_{ox}) or EOT is considered, but they do not provide a clear consideration of these mentioned effects for III-V based MOS devices. Capacitance-equivalent thickness (CET) considers these effects and provides more accurate results. So, that means, less difference between EOT and CET will give us lower quantum effects. Based on this theory, both were calculated for various nanolaminates combination of Al_2O_3 and HfO_2. For the calculation, below equations were used [30]:

$$EOT_{total} = \frac{\varepsilon_0 \varepsilon_{SiO_2}}{C_{ox}}$$

$$EOT_{high-k} = EOT_{total} - T_{SiO_2}$$

$$CET = \frac{\varepsilon_{SiO_2} \times T_{high-k}}{\varepsilon_{high-k}}$$

Fig. 4.1a shows the calculated CET and EOT curves for various nanolaminates and bilayers, where 1:1, 2:6, 3:3 nanolaminates and 1+4 bilayer have the lower difference. Among these, 2:6 has the lowest difference. After analysing this calculation, three samples: 1:1, 2:6 and 3:3 were deposited on an n-type Silicon substrate to check the capacitance-voltage performance, which we can see in **Fig. 4.1b**, **4.1c**, **4.1d**. Because of the high ratio of HfO_2, the 2:6 sample has the highest oxide capacitance. But it also has the highest hysteresis and frequency dispersion for the same reason. In addition, if the hysteresis and frequency dispersion is high then the interface and border traps will also be very high, hence we can not get the suitable performance that we are expecting. For this reason, we decided to omit the 2:6 ratio from our plan. So, finally, we went with 1:1 and 3:3 nanolaminates including a bilayer with the ratio of Al+Hf=1+4 and bare Al_2O_3 for comparison. Table 4.1 shows the deposition process condition on silicon substrate to check the performance. In both, nanolaminates and bilayer, Al_2O_3 is deposited first and then HfO_2.

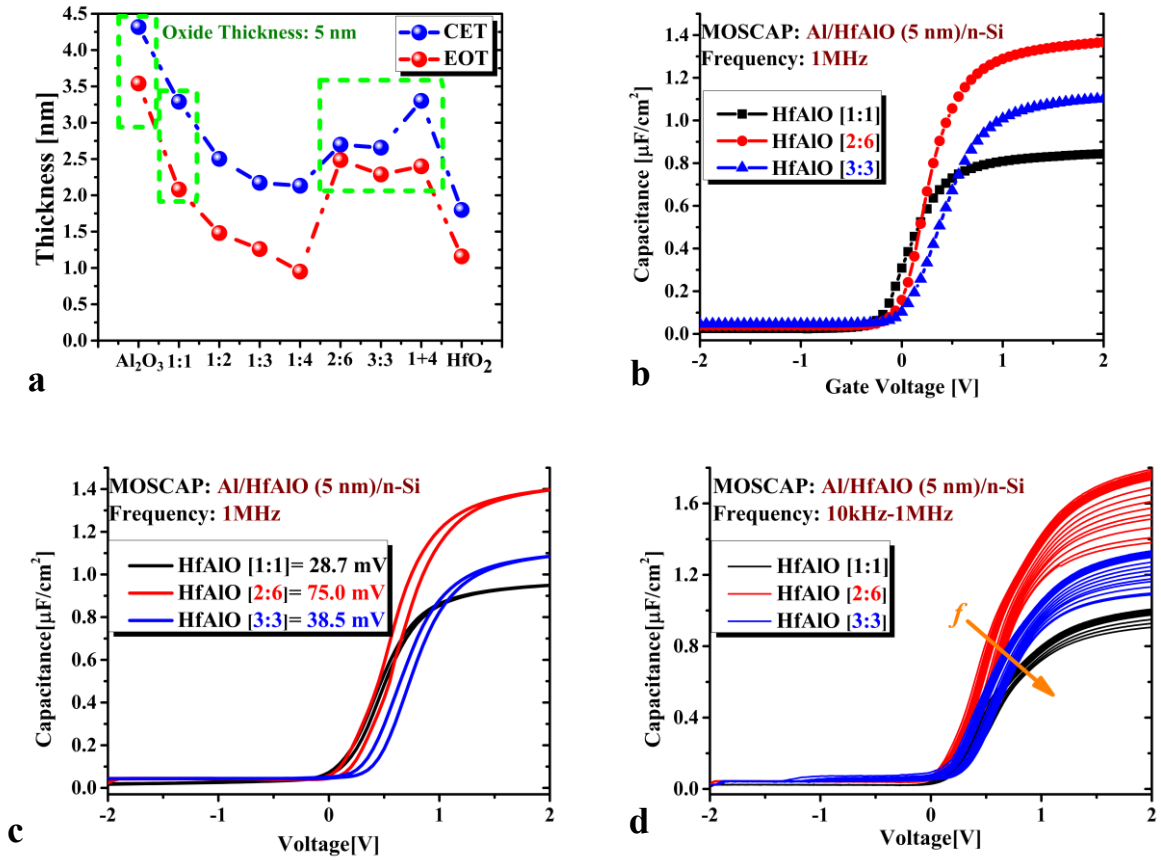

Fig. 4.1 (a) Calculated EOT and CET of various nanolaminates and bilayer; (b) Capacitance Comparison; (c) Hysteresis Comparison; (d) Frequency Dispersion from 10 kHz to 1 MHz.

Table 4.1: Process Information of Oxide Layers in MOSCAP

Split No	Substrate	Process						
		Oxide	Thickness (nm)	TMA	TEMAH	#Super cycles	Purge Gas	ALD Temperature (°C)
Sample#1	n-Si	Al_2O_3	5	**50**			Ar	250
Sample#2		HfAlO=1:1		**1**	**1**	25		
Sample#3		HfAlO=3:3		**3**	**3**	10		
Sample#4		HfAlO=2:6		**2**	**6**	6		
Sample#5		Al+Hf=1+4		**10**	**40**			

Fig. 4.2a is indicating the CET/EOT ratio which demonstrates the difference between CET and EOT for these devices. From the figure we can say that the 3:3 is the nearest to 1.0, that means for 3:3 ratio we have the lowest difference between CET and EOT. Having mentioned that, we also can visualize the marginal difference in terms of CET/EOT among all the samples. Moreover, despite of having a very little difference, the trend between the calculated and measured results are exactly same. **Fig. 4.2b** is showing us the maximum capacitance comparison and obviously because of the HfO_2, 3:3 has the highest capacitance. For the same reason, hysteresis is also high in this sample (in **Fig. 4.2c**) but, if we look at the values of all ratios, 3:3 is not that much high. Therefore, we can expect, applying these ratios into our HEMT structure, will improve the performance compared to Al_2O_3 and other combination.

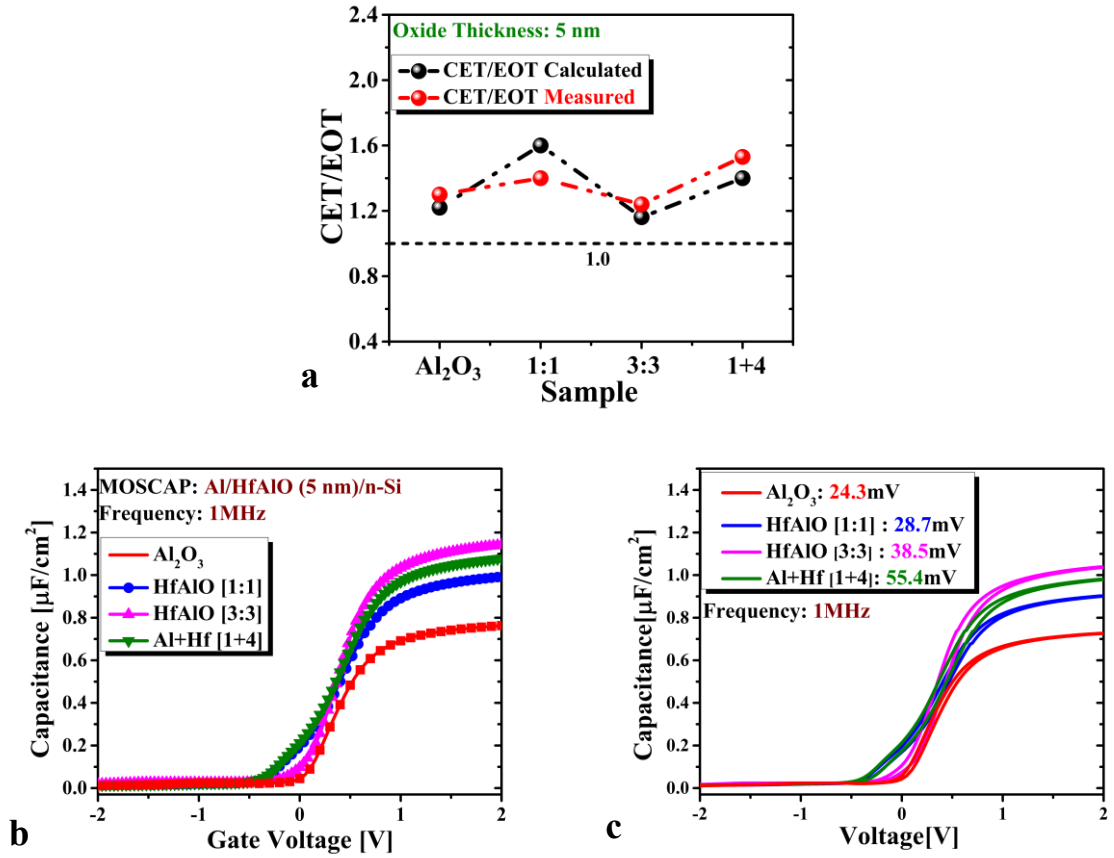

Fig. 4.2 (a) Calculated and Measured CET/EOT of selected combinations; (b) Capacitance Comparison; (c) Hysteresis Comparison;

4.3 Fabrication of MOSHEMT

After analyzing all 4 ratios with MOSCAP, we went for implementing those dielectrics in HEMT to fabricate the MOSHEMT structure. The devices demonstrated in this work was fabricated on a sapphire substrate by metal-organic chemical vapor deposition (MOCVD). The

wafer structure consists of a 2.4-µm GaN buffer layer/150-nm GaN channel layer/20-nm $Al_{0.25}Ga_{0.75}N$ barrier layer. The device fabrication was initiated with solvent cleaning, which was followed by a diluted HCl (10:1) treatment for 5 min. for the removal of surface contaminants and native oxides. Mesa isolation was conducted by induced-coupled plasma (ICP) dry etching using Cl_2/Ar gas mixture. Ti/Al/Ni/Au metal stack was deposited as the source/drain electrode. Then, 30 s of rapid thermal annealing at 850° C was conducted in nitrogen atmosphere to realize the ohmic contact. The atomic layer deposition consisted of Al_2O_3, HfO_2 and its nanolaminate structure according to Al doping ratio. Also, deposition was varied by deposition parameter. After the High-k deposition, a 5 nm of TiN metal was ALD deposited to protect the oxide layer during gate metal deposition. This 5 nm protection of TiN will not affect much in the performance of the MOSHEMT devices, rather, the nitride will give us more solidity in dielectrics. Then the films were treated by liftoff process for gate area modelling. Metal deposition was proceeded for frontside electrode formation. Finally, SF_6 dry etching was done for the removal of TiN layer excluding the metal gate. After MOS-HEMT formation, the devices were characterized by various Parameter analyzer for CV and IV measurements.

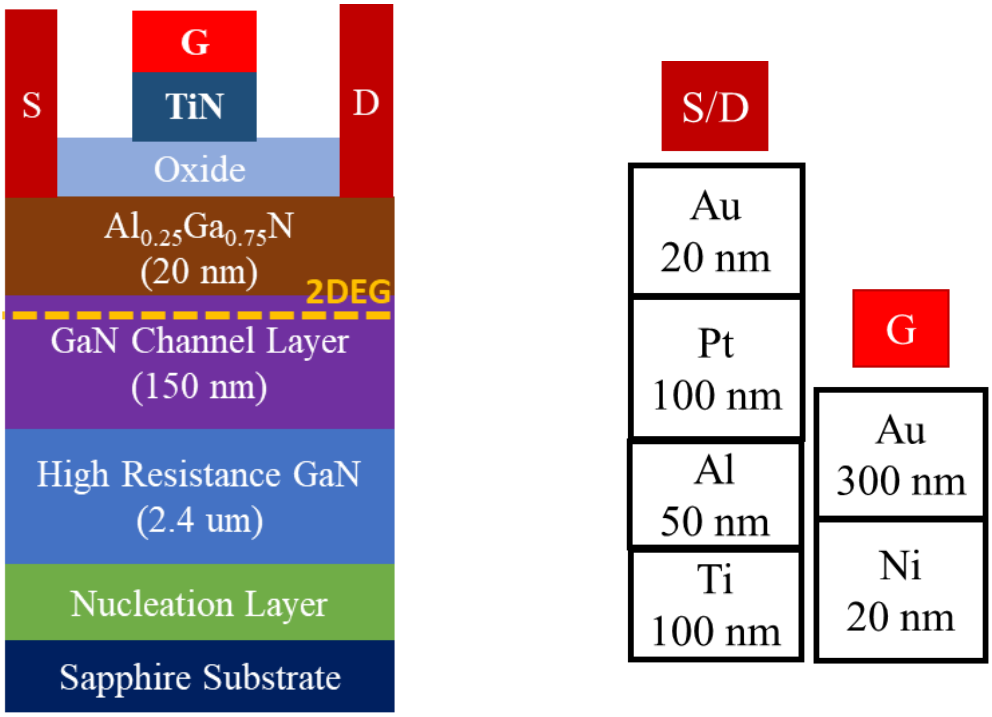

Fig 4.3: Cross sectional structure and layer information of MOSHEMT devices

Table 4.1: Process Information of Oxide Layers

Split No	Substrate	Process						
		Oxide	Thickness (nm)	TMA	TEMAH	#Super cycles	Purge Gas	ALD Temperature (°C)
Sample#1	AlGaN/GaN HEMT	Al_2O_3	5	**50**			Ar	250
Sample#2		HfAlO=1:1	5	**1**	**1**	25		
Sample#3		HfAlO=3:3	5	**3**	**3**	8		
Sample#4		Al+Hf=1+4	5	**10**	**40**			

4.4 Results and Discussion

Fig. 4.4a shows the I_{DS} versus V_{GS} curves of HEMT and MOS-HEMT devices. From a comparison of these device performances, it can be seen that the HEMTs have lower I_{DS} at V_{GS} = 2 & 5 V, compared to the MOS-HEMTs. In this sense, the good quality of both oxides and oxide/HEMT interface has rendered a higher applicable gate bias, which result in a higher driving current capacity of MOS-HEMTs compared to HEMTs. Moreover, the drain current at the same gate bias is also higher for MOS-HEMT. This difference arises, thereby making the MOS-HEMT channel depletion for the same gate voltage smaller than that for the HEMT. Among the MOS-HEMTs HfAlO (3:3) sample has the lowest off state current leakage. This is because of the higher ratio of HfO_2 and Al_2O_3. An interesting fact is that, the threshold voltage has been shifted towards the right side after HfO_2 inclusion in the nanolaminates, about which will be discussed later in brief.

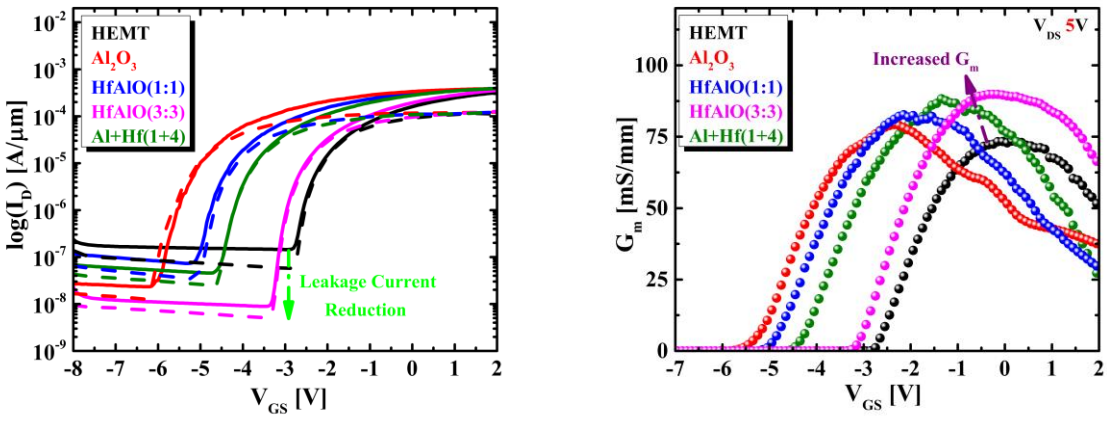

Fig. 4.4 (a)I_{DS} vs. V_{GS} comparison; (b) Evaluation among transconductances for various devices.

Figures 4.4b illustrates the intrinsic transconductance G_m as a function of gate bias for the MOSHEMTs and the HEMT. The combination of higher breakdown voltage and higher drain current imply that the output power of the MOS-HEMT can be much higher that of the HEMT. The peak G_m is around 75 and 90 mS/mm at 14μm gate length for the MOS-HEMT and the HEMT, respectively. Among the MOSHEMTs, transconductance is almost same, but it is still slightly higher for HfAlO (3:3) device. The equation of transconductance is denoted by:

$$G_m = \frac{W}{L}\mu_e C_{ox} V_{DS} \qquad \text{Liner Region}$$

$$G_m = \frac{W}{L}\mu_e C_{ox}(V_{GS} - V_{th}) \qquad \text{Saturation Region}$$

Here, the transconductance is dependent on oxide capacitance C_{ox} and electron mobility μ_e. If these parameters increase then G_m will also increase. So, naturally, using higher dielectric materials in MOSHEMTs will give higher G_m and from the figure it is also found in our case.

Figure 4.5 depicts the gate leakage performance of the both HEMTs and MOS-HEMTs with the same device dimensions, from which the leakage current of MOS-HEMTs is found to be significantly lower than that of the Schottky gate HEMTs. The gate leakage current density of MOSHEMTs is almost 4 orders of magnitude lower than that of the HEMTs. Such a low gate leakage current should be attributed to the large band offsets in the oxide/HEMT and a good quality of all the atomic layer deposited dielectrics and the oxide/HEMT interface. This leads to an increase of the two terminal reverse breakdown voltage (about 25%) and of the forward breakdown voltage (about 30%). At negative bias all the MOSHEMTs have almost same leakage but at positive bias of 2V, the 1+4 bilayer has the lowest. However, the difference between the MOSHEMTs are not that much. Except HfAlO (3:3), it can be said that the variance is very marginal.

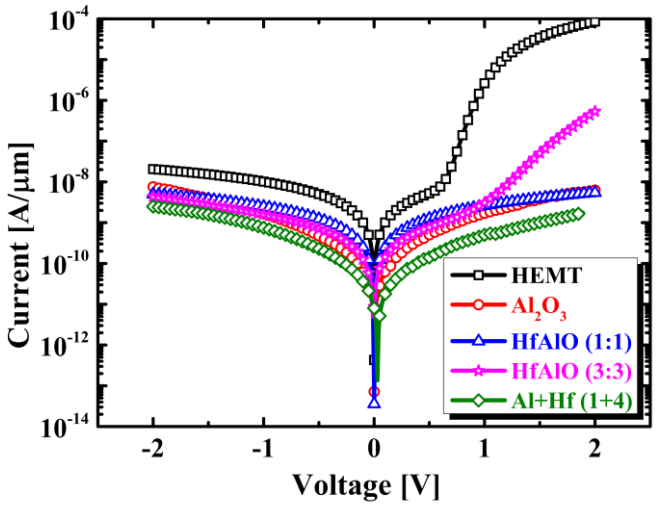

Fig. 4.5 I_{GS} vs. V_{GS} comparison for understanding the gate leakage

Fig. 4.6 shows the output current-voltage (I-V) characteristics of the AlGaN/GaN HEMT and MOS-HEMT. The Schottky-gate device has a maximum drain current of 413 mA/mm^2 at V_{GS} = 2, while the MOS-HEMT devices have around 489 mA/mm^2 drain currents, respectively. Besides, the HEMTs and MOS-HEMTs were completely pinch-off at a gate voltage of -3 and -5V, respectively (not shown here). Moreover, in conventional HEMT, self-heating is higher than the MOSHEMTs. The reason behind self-heating, is phonon scattering which is caused by high electric field of AlGaN. On the other hand, the dielectric constant of a material determines the amount of energy that a capacitor can store when voltage is applied. A dielectric material becomes polarized when it is exposed to an electric field and when polarization occurs, the effective electric field is reduced. So, the higher dielectric constant materials can reduce more electric field as well as phonon scattering. That means, those materials may reduce the self-heating also. Pop et. al. treated all phonon scattering events inelastically, hence, the electrons exchange the correct amount of energy (corresponding to the absorption or emission of a phonon) with each scattering event. Particular attention was paid to the treatment of inelastic acoustic phonon scattering to properly account for energy dissipation at low temperatures and low electric fields [].

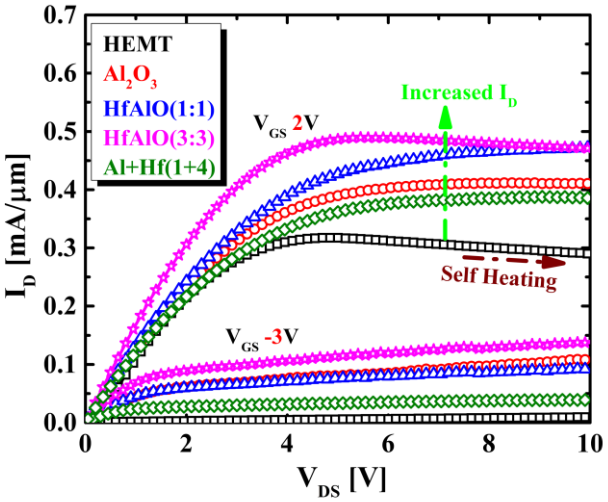

Fig. 4.6 Measured *I–V* characteristics of the MOSHEMT and HEMT.

We used the conductance method for the extraction of interface traps (D_{it}). The conductance method analyses the loss occurred by the change of the trap level charge state. With lower response time τ, traps with an energy level closer to the Fermi level (E_F) can change their occupancy. Walid et. al. showed the equivalent circuit diagram of a transistor in depletion which contains interface traps. C_{ox} is the oxide capacitance, C_s is the semiconductor capacitance and R_s is a series resistance. The C_{it} and G_p represent the equivalent parallel interface trap capacitance and conductance, respectively, which are formed by interface traps. The interface trap capacitance is denoted as $C_{it} = qD_{it}$, where q is the charge of the element and D_{it} is the interface trap density. When electrons are captured by the interface traps, a direct contribution is made to the formation of interface trap capacitance C_{it}. The trap response can be evaluated by the Shockley-Read-Hall statistics of capture and emission rates.

$$\tau = \frac{1}{2\pi f} = \frac{1}{\omega} = \frac{e^{\left(\frac{\Delta E}{K_B T}\right)}}{\sigma v_{th} D_{dos}}$$

So, D_{it} can be calculated from the normalized parallel conductance peak $(G_p/\omega)_{max}$

$$D_{it} \approx \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{\max}$$

Figure 4.7 portrays the interface trap density (D_{it}) of the samples and as-grown sample under different treatment conditions; the trap density was calculated with the conductance method by considering the series resistance correction with the above equation. For HEMT Dit value is found around 4×10^{12} region whereas, because of the oxide layer and oxide/HEMT trapping, in MOSHEMT, the value is between 1.6×10^{13} and 6.5×10^{13}. Predominantly, interface traps increased with the HfO_2 inclusion in the nanolaminates, which is because HfO_2 has higher hysteresis and dispersion in the depletion region than Al_2O_3.

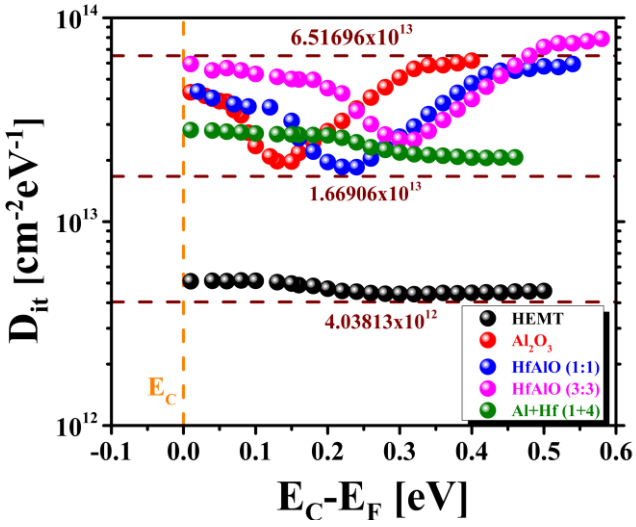

Fig. 4.7 Interface Trap Density of the MOSHEMTs and HEMT.

For border trap extraction, we used the distributed circuit model. Generally, the border traps in the insulator and the mobile carriers in semiconductor bands can exchange charge. Usually this charge exchange occurs through tunneling. The average time for an empty trap to capture electron is denoted by τ, which is exponentially proportional to the distance x between the trap and interface. Here, τ_0 represents capture/emission time constant and k is the attenuation coefficient. The effective mass of the insulator is denoted by m*, E_b is the barrier height between the insulator and semiconductor conduction bands.

$$\tau = \tau_0 e^{2kx} \quad \text{where,} \quad k = \frac{\sqrt{2m^* \times E_b}}{\hbar}$$

$$\tau_0 = \left(n_s v_{th} \sigma \right)^{-1}$$

Here, n_s is the electron density of the semiconductor surface, v_{th} is the electron thermal velocity, and σ is the capture cross-section area of the border trap. When the device is in accumulation, the Fermi level is close to the conduction band. In this situation, n_s can become relatively equal to the density of states of the conduction band.

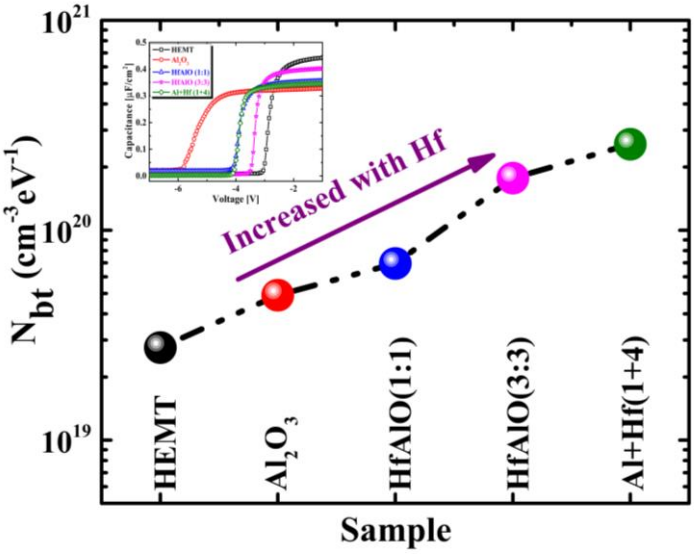

Fig. 4.8 Border Trap Density of the MOSHEMTs and HEMT.

Fig. 4.8 is showing the border trap comparisons among MOSHEMTs and HEMTs. The value ofNbt is increased after oxide layer inclusion. Similar as Dit, trapping is higher with more Hf in the nanolaminates and bilayer. In HEMT, the value is found around 2.7×10^{19} cm^{-3}eV^{-1}; whereas, it is increased as 4.9×10^{19}, 6.9×10^{19}, 1.7×10^{20}, 2.6×10^{20} cm^{-3}eV^{-1} for Al_2O_3, HfAlO (1:1), HfAlO (3:3) and Al+Hf (1+4) respectively. This reduction may be attributed to the remote selective oxygen scavenging phenomenon of Al_2O_3. In nanolaminate film at the time of Al_2O_3 ALD deposition, the excess TMA precursor after the surface hydroxyl group elimination, it reduces the additional species which are either out diffused through HfO_2 or remotely at the deposition surface. The inset figure is stating the maximum capacitance values, where also HfAlO (3:3) is the highest one. In bilayer, two different materials are combined in series; therefore, their capacitance are also added in series. Now, the capacitance formula for series connection is:

$$C_{tot} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}}$$

So, because of this equation, the capacitance of bilayer will be lower than nanolaminates. In nanolaminates, both materials are not added in a series, rather, those are bonded together.

4.5 Conclusion

This work has given a demonstration of the characteristics of atomic-layer-deposited aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2) nanolaminates and bilayers on an n-type silicon (n-Si) substrate altered by Al_2O_3 and HfO_2 deposition cycles. Theory and measurement-based calculations were used to calculate capacitance equivalent thickness (CET) and equivalent oxide thickness (EOT). Based on the results of the basic capacitance voltage (C-V) properties, four combinations, including Al_2O_3, were chosen to be implemented in the aluminium gallium nitride/gallium nitride high electron mobility transistor (AlGaN/GaN HEMT) structure to create metal oxide semiconductor high electron mobility transistors (MOSHEMT). Different DC properties were extracted where the AlGaN/GaN HEMT had a high leakage current and a low transconductance issue. MOSHEMTs, on the other hand, delivered greater performance, and all of the process conditions as well as attributes were addressed with good rationale. Compared to Al_2O_3, the nanolaminates and bilayers performed better as dielectrics. Here, in this work, we have optimized MOSHEMTs by evaluating various combinations of Al_2O_3 and HfO_2 nanolaminates and their bilayer.

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Chapter 6: Conclusions and future works

6.1 Conclusion

In this study, the characteristics of Al_2O_3 PDA-annealed under different conditions on Si substrate were investigated. The results clearly indicate that the annealed samples show better characteristics than the non-annealed samples. Moreover, the diffusion properties of the silicon and oxide layers were discussed. This article divulges an unopened scenario and also presents the optimal conditions for post deposition annealing of Al/Al_2O_3/n-Si stacks. Then the characterization of MOSHEMT was carried out at four different Al_2O_3 and HfO_2 ratios including conventional HEMT and Hf dominant MOSHEMTs showed higher trapping phenomena. HfAlO (3:3) sample showed the highest transconductance, lowest off state leakage current, moderate gate leakage, highest output drain current and capacitance value. The performance difference among the MOSHEMTs are very marginal. All the attributes and process conditions were described briefly with various figures and equations for understanding the optimization of Al_2O_3 and HfO_2 nanolaminates in AlGaN/GaN High Electron Mobility Transistor.

6.2 Suggestions for future works

- ✓ To check the RF characteristics along with Noise parameter and Pulsed IV.
- ✓ To use other materials like TiO_2 in nanolaminates and bilayer.
- ✓ To study about Maxwell -Wagner (M-W) instability for the case of bilayer and single layered high-*k* structure.