**Doctor of Philosophy**

# Optimization of GaN-Based High-Electron-Mobility Transistors (HEMTs) for High-Frequency Applications: A Comprehensive Study on Reliability and Performance Enhancement

The Graduate School
of the University of Ulsan
Department of Electrical,
Electronic and Computer Engineering

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# Optimization of GaN-Based High-Electron-Mobility Transistors (HEMTs) for High-Frequency Applications: A Comprehensive Study on Reliability and Performance Enhancement

Supervisor: Prof. Sunghwan Kim

A Dissertation

Submitted to
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Doctor of Philosophy

by

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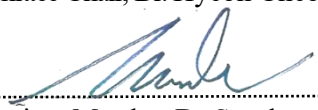

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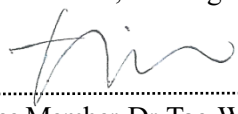

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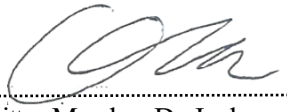

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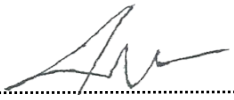

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**ABSTRACT**

The widespread application of GaN-based high electron mobility transistors (HEMTs) in high-frequency and high-power applications still faces reliability instability. Achieving the necessary reliability is a challenging problem, primarily attributed to the elevated operational voltage and material properties. To enhance reliability, it is crucial to develop a comprehensive physical understanding of the underlying degradation mechanisms. This comprehensive thesis undertakes an in-depth exploration of trapping-related degradation in AlGaN/GaN high electron mobility transistors (HEMTs), extending and refining prior research on structural issues. The investigation encompasses a multi-faceted approach, beginning with a thorough characterization of interface and border traps using frequency-dependent C-V and G-V methods. The study then explores the influence of Al composition in AlGaN barriers on device performance, revealing insights into trap densities and their implications. A novel aspect of the research involves the application of $O_2$ plasma treatment to mitigate volume trap states, showcasing improvements in Schottky characteristics and microwave performance. Additionally, the thesis provides a thorough analysis of Positive-Bias-Temperature Instability (PBTI) and the impact of channel back-barrier and channel thickness scaling, explaining the intricate relationship between these factors. Overall, this research significantly advances our understanding of trapping effects in AlGaN/GaN HEMTs, proposing innovative strategies to enhance device reliability and performance across various operational conditions.

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# Chapter 1

# Introduction

## 1.1 III-V Compound Semiconductor

III-V transistors, particularly those based on compound semiconductors, have a fascinating history and pivotal contributions to the field of electronics. The III-V semiconductor materials consist of elements from groups III and V of the periodic table. The most common compound semiconductors in this category are made from elements like gallium (Ga), indium (In), and aluminum (Al) from group III combined with nitrogen (N), phosphorus (P), arsenic (As), or antimony (Sb) from group V.

The development of III-V compound semiconductors, particularly gallium arsenide (GaAs), played a crucial role in the evolution of transistors[1]. GaAs has exceptional electrical properties that allow for high-frequency operation, making it suitable for radiofrequency applications[2]. In the 1970s and 1980s, GaAs-based transistors gained prominence in the industry, especially for high-frequency and high-power applications, due to their faster switching speed and power handling capabilities compared to silicon-based transistors.

One of the significant advancements was the invention of the high electron mobility transistor (HEMT) in the late 1970s and early 1980s. HEMTs, also known as modulation-doped field-effect transistors (MODFETs), are crucial components in radiofrequency amplifiers, microwave devices, and high-speed integrated circuits[3]. They utilize III-V materials like GaAs and InP (Indium Phosphide) and offer high electron mobility, making them highly suitable for high-frequency and high-speed applications.

Over time, other III-V materials like InP (Indium Phosphide) and GaN (Gallium Nitride) have emerged, contributing to advancements in semiconductor technology[4][5]. Gallium Nitride transistors, in particular, have demonstrated their potential in power electronics, RF amplifiers,

and even in optoelectronic applications like LEDs and laser diodes.

The evolution of III-V semiconductor technology has been a crucial part of the development of compound semiconductor devices. Their capabilities in high-frequency operation, power handling, and efficiency have expanded their use in various applications, including telecommunications, satellite communications, radar systems, and more, and continue to be an area of active research and development.

### 1.2 GaN High Electron Mobility Transistors

Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) represent a critical breakthrough in semiconductor device technology. This class of transistors is built from gallium nitride, a robust wide-bandgap semiconductor material with remarkable electrical properties. GaN HEMTs have garnered significant attention due to their potential for high-power, high-frequency applications. The exceptional characteristics of GaN, with its high band-gap (measuring at 3.4 eV), enable GaN-based devices to endure remarkably high voltages[6]. Demonstrations have shown GaN-based devices with a notably high breakdown voltage reaching 8300 V[7]. Moreover, the III-nitride material's piezoelectric effect and spontaneous polarization facilitate a high sheet carrier density, surpassing $10^{13}$ $cm^{-2}$ in AlGaN/GaN heterostructures without the need for conventional doping[8][9]. This attribute translates to easily attainable high current density within GaN HEMTs. The combination of its high voltage handling capability and the capacity for high current density render GaN HEMTs exceedingly suitable for high-power applications.

Furthermore, the significant conduction band discontinuity between AlGaN and GaN results in the AlGaN/GaN structure exhibiting a high electron mobility (exceeding 2000 $cm^2$/V-s) and an exceptionally high electron saturation velocity (measured at $2.5x10^7$ cm/s)[10][6]. These features pave the way for high-frequency and high-power operations, highlighted by the demonstration of an $f_T$ (Unity current gain cutoff frequency) of 454 GHz and $f_{max}$ (Maximum oscillation frequency) of 554 GHz using a 20 nm ‘T’ gate device with a 100% Al in the AlGaN barrier and $n^+$ GaN source/drain contact[6]. The unique material properties of GaN bestow AlGaN/GaN HEMTs with exceptional performance across a wide range of frequencies in RF power applications. Impressively, demonstrations have showcased an output power density of 40

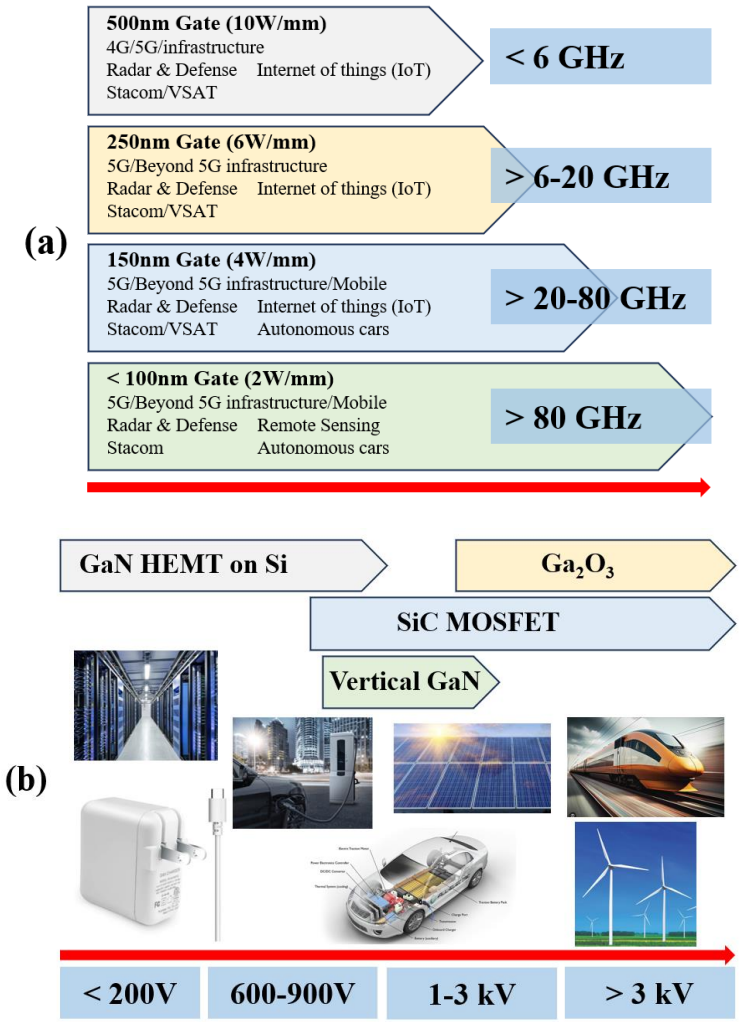



**Figure 1-1 (a)** A technology roadmap for RF GaN HEMTs. **(b)** A technology roadmap for Power GaN HEMTs.[11]

W/mm at 4 GHz, 13.7 W/mm at 30 GHz, and 2.1 W/mm at 80.5 GHz, eclipsing the capabilities of conventional technologies reliant on GaAs or InP[12][13][14]. GaN HEMTs exhibit unparalleled performance, offering substantial promise for applications demanding high-power, high-frequency functionality, such as WLAN base stations and high-voltage switching applications in power electronics. The roadmap in GaN HEMTs applications is illustrated in figure 1-1.

### 1.3 Motivation

A major challenge currently constraining the widespread adoption of GaN HEMT technology is its constrained device performance due to electrical reliability. Despite notable advancements in the reliability of GaN HEMTs in recent years, these devices continue to contend with various degradation mechanisms[15][16]. Consequently, GaN HEMTs have not yet achieved robust reliability in both RF and DC applications. For instance, figure 1-2 shows the drain current degradation observed in AlGaN/GaN HEMT devices during pulsed *I-V* measurement, an experiment conducted within this study. The measurement involved applying a single short pulse in the gate, recording $V_G$ pulse and its corresponding $I_D$ response, which were then transformed into $I_D$–$V_{GS}$ or $I_D$–*time* curves. Notably, hysteresis and drain current degradation over time due to charge trapping within the AlGaN barrier were observed. These trapping phenomena lead to a decline in device performance, posing a significant challenge, particularly for applications such as satellite communications, which demand exceptionally high reliability. Given that these devices are designed for high-frequency, high-power, and high-voltage applications and are expected to operate at high temperatures due to GaN's high band-gap, ensuring solid device performance becomes particularly challenging in extreme operating environments without robust reliability.

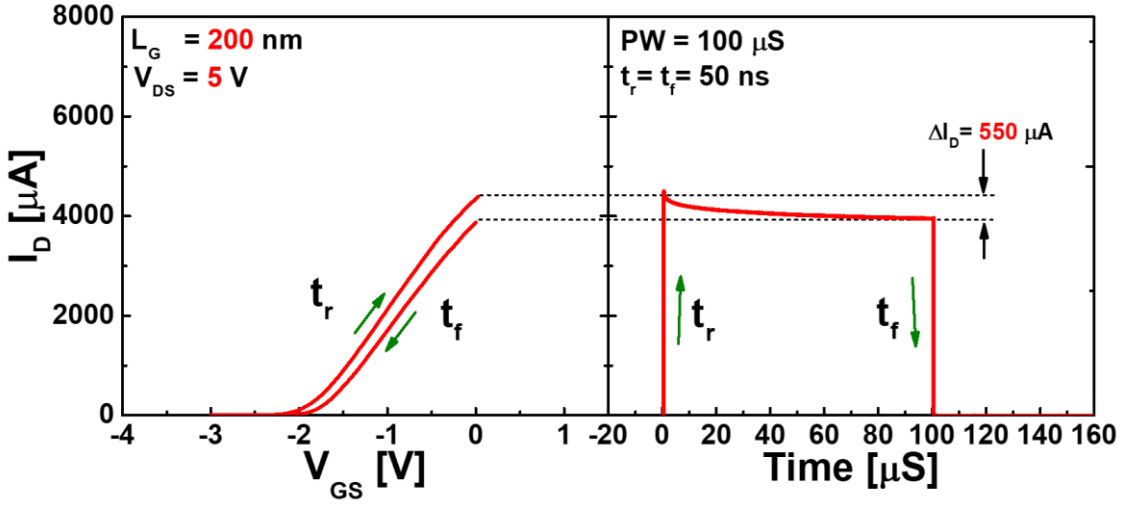



**Figure 1-2** Pulsed $I_D$ vs $V_{GS}$ and $I_D$ vs. pulse time showing $\Delta I_D$ degradation due to charge trapping.

In order to achieve consistent device performance with robust reliability, it requires a comprehensive understanding of the underlying physical mechanisms behind device degradation. This involves understanding how normal or stressed operational conditions—such as current, voltage, temperature, and environmental factors—contribute to degradation. It is vital to identify which device performance parameters ($I_D$, $G_m$, $V_T$) degrade, the process of degradation, and the influence of device design, encompassing device geometry and heterostructure. Furthermore, as there's typically a trade-off between performance and reliability, a comprehensive grasp of the degradation's physics allows for the strategic design of device structure and heterostructure to achieve an optimized balance between performance and reliability. Additionally, understanding the physical degradation mechanism is critical for assessing device reliability. Defect sites within the epitaxial layers stand as the primary reason behind the degradation of GaN HEMTs, actively capturing and emitting channel electrons during device operation. These trapping phenomena intensify under stressed conditions, typically evaluated to determine device reliability. A profound comprehension of the physical mechanisms behind charge trapping is pivotal for enabling the proper scalability of GaN HEMTs, and facilitating performance enhancement.

To date, numerous hypotheses have emerged to elucidate the degradation of GaN HEMTs. Prominent among these theories are hot-electron-induced trap formation, hot electron trapping at the surface, and the development of crystallographic defects via the inverse piezoelectric effect[15][16][17]. However, our comprehension of device degradation remains incomplete, necessitating a more intricate understanding of these mechanisms and the discovery of potential yet-unidentified degradation pathways. Moreover, the development of novel measurement techniques tailored to investigate diverse phenomena within GaN HEMTs is imperative for achieving a deeper insight into these degradation mechanisms.

In this thesis, we delve into the intricate physical mechanisms underlying the degradation of AlGaN/GaN HEMTs by employing an array of device characterization techniques. Our objective is to shed light on pathways for enhancing device scalability while concurrently improving device reliability.

## 1.4 Objectives

This thesis encompasses a comprehensive investigation into the physical mechanisms of trapping-related degradation in AlGaN/GaN high electron mobility transistors (HEMTs), seeking to advance device reliability and performance.

1. The primary objective revolves around scrutinizing the impact of trapping effects on device performance, understanding trapping mechanisms within the AlGaN barrier and AlGaN/GaN interface as well as the impact of Al composition in the AlGaN barrier.

2. Secondly, evaluating the influence of various structural modifications on these devices. Exploring the impact of $O_2$ plasma treatment on the surface as well as the volume trap states within the AlGaN barrier layer, focusing on the scaling down of channel thickness, the impact of the $Al_{0.08}Ga_{0.92}N$ channel back barrier.

These objectives have been approached through a multi-faceted reliability analysis, incorporating frequency-dependent *C-V* and *G-V* methods, pulsed *I-V* characterizations, low-frequency 1/*f* noise characterizations, and Positive-Bias-Temperature Instability (PBTI). The intent is to establish a deeper understanding of these trapping mechanisms, and their impact on device reliability and scalability, and to propose measures to enhance device performance without compromising reliability. The work aims to contribute insights and strategies that can propel the advancement of AlGaN/GaN HEMTs in high-power, high-frequency applications while ensuring their long-term reliability and robust performance.

## 1.5 Thesis outline

The thesis is structured as follows: Chapter 2 presents background information on GaN-based HEMTs, discussing key technologies and reliability issues related to high-performance GaN HEMTs.

Chapter 3 offers an overview of the AlGaN/GaN HEMTs utilized in this study, delving into the fabrication process and detailing the chip designed specifically for this research. Additionally, the chapter comprehensively explains the various reliability characterization methods employed throughout the study. These methods encompass interface and border trap characterization,

volume trap density extraction, low-frequency noise characterizations, the pulsed *I-V* technique, and the methodology for stress characterizations.

Chapter 4 provides an in-depth overview of the extraction of interfacial trap densities in AlGaN/GaN HEMTs. It reports, for the first time, the use of conventional frequency-dependent C-V and G-V methods to characterize the interface trap density ($D_{it}$) between AlGaN and GaN and the deep-level/border trap density ($N_{bt}$) in the AlGaN barrier layer in a long-channel AlGaN/GaN HEMT fabricated on a SiC substrate. The primary focus was on the trap states inside the AlGaN layer, situated at the interface and near the interface of the AlGaN/GaN, with attempts made to eliminate other potential interfacial trap-contributing factors, such as dielectric layers for passivation.

In Chapter 5, an in-depth trapping characteristic analysis of the $Al_xGa_{1-x}N$/GaN interface of AlGaN/GaN HEMTs based on the variation of Al composition in the $Al_xGa_{1-x}N$ barrier and its effects on device performance was presented. It demonstrates that trapping effects, significantly impacting device performance, are primarily influenced by the quality of the interface between the AlGaN and GaN layers.

Chapter 6 analyzes in detail the effect of employing $O_2$ plasma treatment before the deposition of the gate metal on top of an AlGaN layer. It demonstrates that the $O_2$ ions not only passivated the AlGaN gate surface area but also penetrated into the bulk, forming Al–O and Ga–O bonds, while treating the volume trap states. Additionally, RF gm collapse effects were improved, ultimately increasing the microwave output performance.

Chapter 7 introduces structural modifications, such as the inclusion of an AlGaN channel back barrier and channel thickness scaling to improve device performance. Positive Bias Temperature Instability (PBTI) and its correlation with trapping effects, responsible for device instabilities, are extensively explored. These modifications are demonstrated to significantly improve $f_T$ and $f_{max}$ of the devices.

Finally, Chapter 8 concludes by summarizing the research findings and proposing guidelines for enhancing reliability in device design. Additionally, it provides recommendations for future research.

# Chapter 2

# Fundamentals of GaN HEMTs

## 2.1 GaN material properties

Gallium Nitride (GaN), a wide-bandgap semiconductor, has garnered considerable attention in the field of electronics due to its unique material properties that make it exceptionally well-suited for high-power, high-frequency applications. This semiconductor's distinct characteristics set it apart from others and position it as a key material for the next generation of electronic devices.

One of the standout features of GaN is its wide energy gap, measuring approximately 3.4 eV[18]. This energy gap is more than three times that of silicon (Si). The significance of this wide energy gap lies in its ability to withstand high electric fields. GaN exhibits a high breakdown electric field of 3.3 MV/cm, making it a robust choice for high-power and high-frequency applications that often require operation at elevated temperatures[6]. As a result, GaN has found extensive use in both commercial and military markets.

GaN's remarkable electron mobility, which measures approximately 900 $cm^2/V \cdot s$, is another defining property. This high electron mobility, combined with GaN's capacity to handle high voltages, allows for higher saturation velocities, reaching up to 2.7 x $10^7$ cm/s[18]. These properties are instrumental in enhancing operating frequencies, making GaN-based devices well-suited for high-frequency applications.

In addition to its electronic properties, GaN also exhibits excellent mechanical and thermal stability. This, along with its good thermal conductivity, makes GaN an ideal choice for dissipating heat. Devices fabricated on silicon carbide (SiC) substrates, using GaN, can operate at higher temperatures and power levels, which is crucial for many applications. Comparing the key material properties of GaN with other well-known semiconductors, such as silicon (Si), highlights GaN's unique advantages. Here is a table that compares the basic material properties

of GaN with other well-known semiconductors:

**Table 2-1** Comparison of physical properties of various semiconductors for high-voltage applications[18].

| Material Properties | Si | 6H-SiC | GaAs | GaN |
|---|---|---|---|---|
| Bandgap Energy (eV) | 1.1 | 3.0 | 1.43 | 3.4 |
| Electron Mobility ($cm^2/V \cdot s$) | 1400 | 400 | 8500 | 900 |
| Saturated (Peak) Drift Velocity (x $10^7$ cm/s) | 1.0 | 2.0 | 2.1 | 2.7 |
| Breakdown Electric Field (MV/cm) | 0.3 | 2.4 | 0.4 | 3.3 |
| Thermal Conductivity (W/cm·K) | 1.5 | 4.5 | 0.5 | 1.3 |
| Relative Dielectric Constant | 11.8 (static) | 9.7 (HF) | 6.7 (static) | 12.9 (static) |

These properties collectively highlight GaN as a standout material for high-power, high-frequency applications. Its wide energy gap, high electron mobility, and excellent thermal characteristics contribute to its superior performance.

Figure 2.1 provides a comparison among GaN, Si, and GaAs, highlighting their respective advantages in RF and power supply circuits. It illustrates that GaN stands out as the primary material for the upcoming generation of high-frequency, high-power, high-voltage, high-temperature, and low-loss operating specification transistors[18]. Hence, GaN is deemed an excellent and prominent candidate for high-performance HEMTs.

GaN's potential as a high-performance semiconductor is further reinforced by two key figures of merit:

- Johnson's Figure of Merit (JFOM) assesses a device's ability to operate at both high power and high frequency. It is calculated as the product of electric field breakdown ($E_C$) and electron saturation velocity ($V_S$). Higher JFOM values indicate a device's enhanced capability to handle high power and high-frequency operation[19].

$$JFOM = \frac{E_C V_S}{2\pi} \tag{2.1}$$

- Baliga's Figure of Merit (BFOM) gauges the resistive losses of a device and is vital for evaluating the performance of power electronic devices. It is determined by factors such as the dielectric constant ($\varepsilon$), carrier mobility ($\mu$), and the critical breakdown field ($E_C$) of the semiconductor[20].

$$BFOM = \in \mu E_C^3 \tag{2.2}$$

When comparing these figures of merit, GaN outperforms traditional semiconductors by a significant margin.

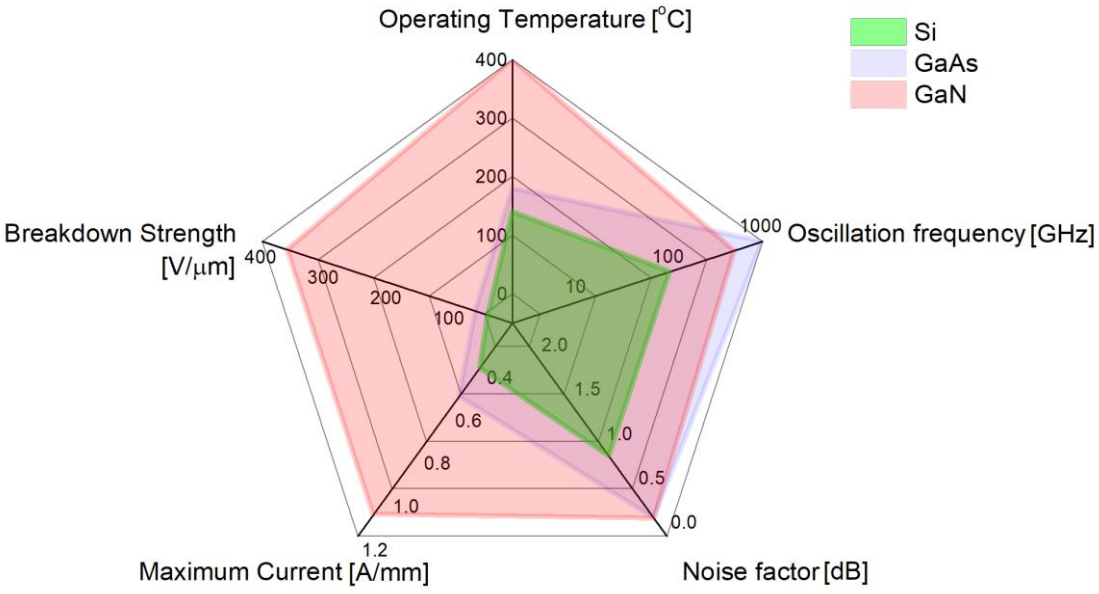



**Figure 2-1** Comparison of GaN material merits to Si and GaAs.

Table 1.2 presents a comparison between GaN and conventional semiconductor materials. The figures of merit are normalized concerning those calculated for silicon (Si) material. Higher values indicate greater desirability. The comparison outlines the Johnson Figure of Merit (JFOM) and Baliga Figure of Merit (BFOM) for Si, GaAs, and GaN materials[21]:

**Table 2-2** Comparison of JFOM and BFOM for Si, GaAs and GaN materials[21].

| Material | JFOM/JFOM (Si) | BFOM/BFOM (Si) |
|---|---|---|
| Si | 1 | 1 |
| GaAs | 1.8 | 14.8 |
| GaN | 215.1 | 186.7 |

In summary, GaN's wide energy gap, high electron mobility, high saturation velocity, and excellent thermal properties make it an ideal candidate for high-performance HEMTs and other electronic devices. Its figures of merit demonstrate that GaN surpasses traditional semiconductors, positioning it as a key material for the next generation of high-frequency, high-power, high-voltage, high-temperature, and low-loss electronic devices.

## 2.2 AlGaN/GaN High Electron Mobility Transistors

AlGaN/GaN HEMT epitaxy techniques encompass molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD)[22][23]. While MBE-grown devices showcase a performance comparable to those produced through MOCVD[24], the long-term cost efficiency favors MOCVD over MBE for commercial AlGaN/GaN HEMT growth. Both AlN and GaN exhibit a wurtzite-type hexagonal crystal structure[25]. GaN epitaxy comes in two forms based on the cut-face: Ga-polar and N-polar. Typically, Ga-polar film is grown using MOCVD, while N-polar film is cultivated by MBE under specific conditions[26]. The devices analyzed in this study are Ga-polar AlGaN/GaN HEMTs. Due to the higher electronegativity of nitrogen compared to gallium and aluminum, GaN and AlN demonstrate strong spontaneous polarization, measuring 0.029 and 0.081 C/m², respectively[27]. Additionally, these materials exhibit piezoelectric polarization as piezoelectric substances. When a thin layer of $Al_xGa_{1-x}N$ is grown atop Ga-polar GaN, it undergoes tensile strain, resulting in piezoelectric polarization aligned with the spontaneous polarization (Figure 2-2 b). This substantial polarization generates an electric field within the AlGaN layer.

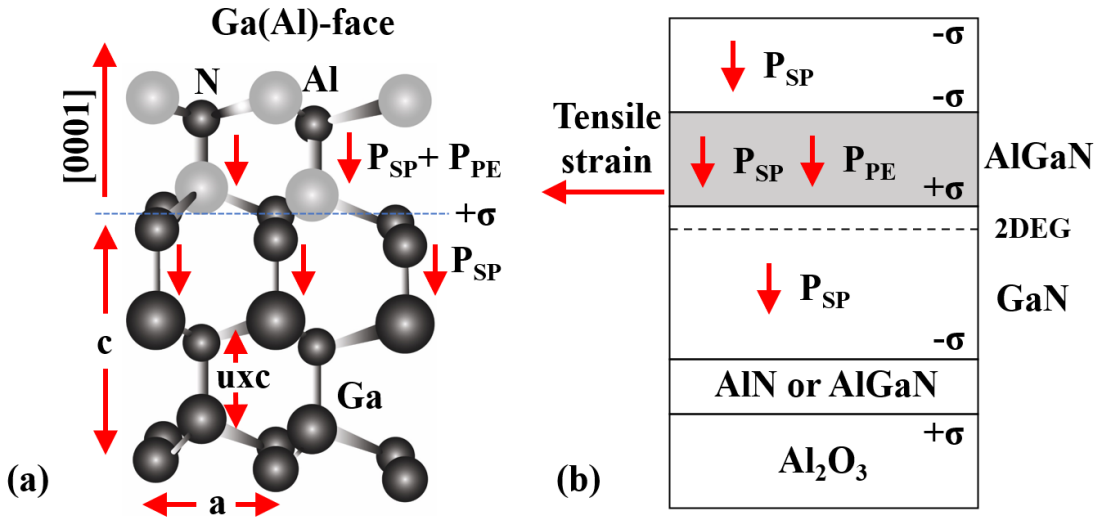



**Figure 2-2 (a)** the Ga-polar GaN crystal structure and **(b)** the presence of spontaneous and piezoelectric polarization within the Ga-polar system, featuring the 2DEG situated at the lower AlGaN/GaN interface[28].

In unintentionally doped AlGaN, it is assumed that surface donor states exist at the top of the AlGaN layer. When the AlGaN layer reaches a sufficient thickness for the Fermi level to access these states, electrons are stimulated to transition into the conduction band. Guided by the electric field, these electrons move towards the AlGaN/GaN interface. Upon reaching the GaN layer, these electrons flow into the GaN side due to its lower Fermi level. This flow continues until the Fermi level equalizes, establishing a 2-dimensional electron gas (2DEG) at the AlGaN/GaN interface[29]. These electrons are confined at the interface, as illustrated in Figure 2-3, yet exhibit high mobility within the AlGaN/GaN interface. Tuning the Al molar fraction x and the thickness of $Al_xGa_{1-x}N$ can further boost the carrier sheet density and mobility in the 2DEG. An increase in the Al molar fraction and $Al_xGa_{1-x}N$ thickness augments the carrier sheet density by elevating the piezoelectric polarization. However, this elevation often results in decreased carrier mobility due to increased scattering when the carrier density rises[30].

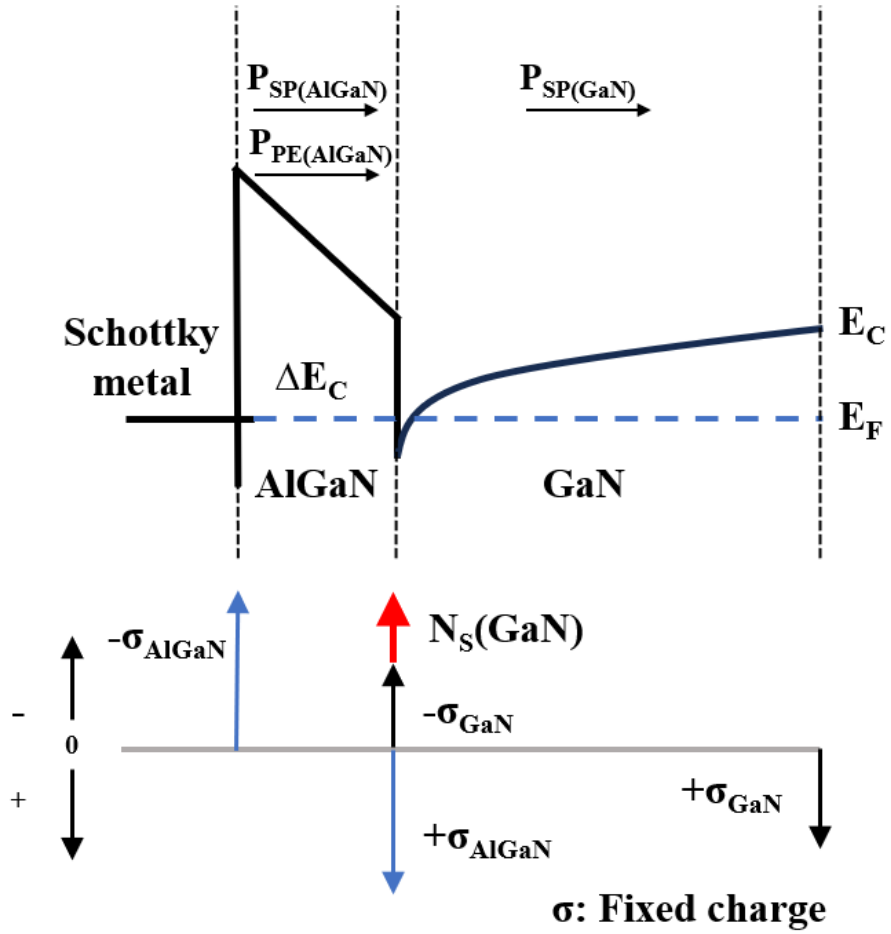



**Figure 2-3** The energy band diagram and charge distribution illustration of a Ga-polar AlGaN/GaN HEMT in its unbiased state[31].

### 2.3 Substrates

Due to the high cost of GaN substrates, AlGaN/GaN HEMTs are commonly cultivated on alternative substrates such as sapphire, SiC, and Si. Each substrate's properties concerning GaN epitaxy are detailed in Table 2-3. Among these substrates, SiC exhibits the most favorable compatibility with AlGaN/GaN epitaxy, albeit being the most expensive. The more cost-effective alternatives include sapphire or Si, with Si displaying more promising characteristics compared to sapphire. Si substrates are available in larger sizes of up to 12 inches and experience fewer issues with wafer-bow management compared to sapphire[32]. AlGaN/GaN epitaxy is predominantly grown on (111) Si due to its trigonal symmetry, facilitating the epitaxial growth of (0001) GaN[33]. Moreover, growing AlGaN/GaN on Si enables seamless integration between AlGaN/GaN HEMT and Si-based semiconductors[34][35][36]. This integration fosters cost-

effective large-scale production and paves the way for innovative applications. Despite these prospects, there remain numerous reliability issues that demand attention[17]. Consequently, this project endeavors to advance the understanding of the reliability of AlGaN/GaN HEMT-on-Si.

**Table 2-3** Comparison of substrate properties

| Properties | Sapphire | SiC | Si | GaN |
|---|---|---|---|---|
| Lattice mismatch (%) | 16 | 3.1 | -17 | 0 |
| Linear thermal expansion coefficient ($\times 10^{-6}$ $K^{-1}$) | 7.5 | 4.4 | 2.6 | 5.6 |
| Thermal conductivity (W $cm^{-1}$ $K^{-1}$) | 0.25 | 4.9 | 1.6 | 2.3 |
| Cost | Cheap | Expensive | Cheap | Very Expensive |
| Dislocation density of GaN film ($cm^{-2}$) | $10^8$ | $10^8$ | $10^9$ | $10^4$-$10^6$ |

## 2.4 Failure Mechanism

GaN HEMTs present distinctive reliability challenges associated with material properties and the quality of epitaxial growth[37][38][15][39]. In Figure 2-4, a schematic cross-section of an AlGaN/GaN HEMT is depicted, outlining primary failure mechanisms reported in the literature. These are briefly summarized below. The primary objective is to spotlight some of the most recent findings that are pertinent to state-of-the-art devices and future advancements.

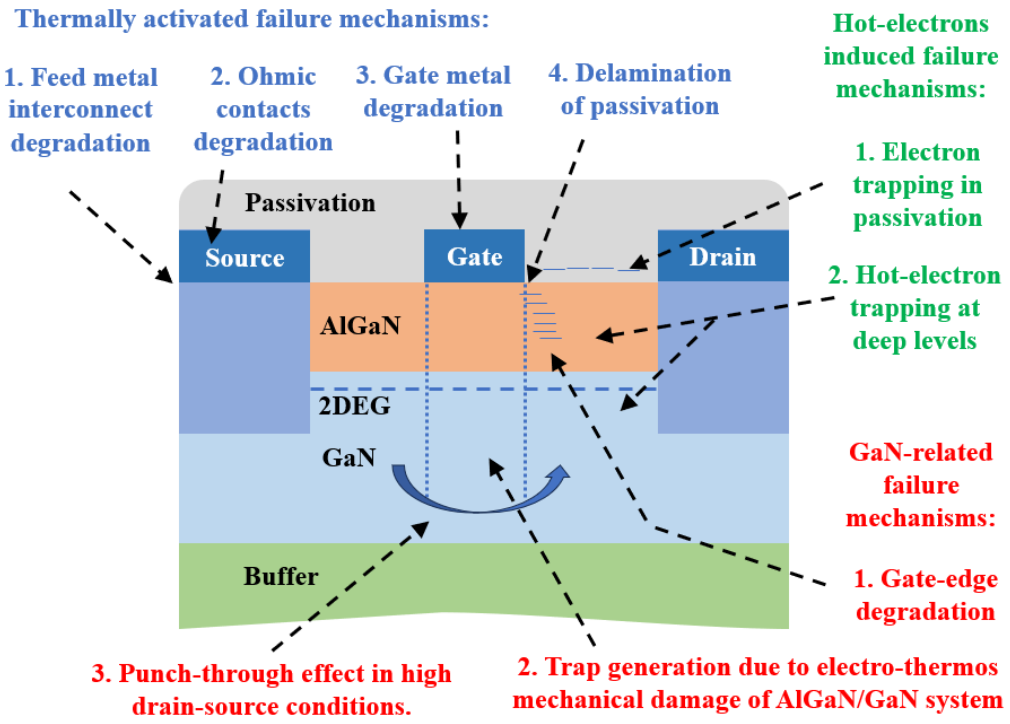



**Figure 2-4** Illustrative diagram depicting the primary mechanisms influencing the reliability of GaN-based High Electron Mobility Transistors (HEMTs)[16].

### 2.4.1 Inverse Piezoelectric Effect and Thermo-mechanical Strain

The most sensitive region in a GaN HEMT is situated in the semiconductor layers near the gate's drain-side edge, where high current density, electric field, and localized temperature coincide. At this specific location, various degradation mechanisms are expedited: the piezoelectric properties of GaN lead to amplified tensile stress within the AlGaN barrier due to the presence of an electric field. This stress relief often generates lattice defects or cracks, resulting in the decline of drain current ($I_D$) and an upsurge in gate leakage current ($I_G$). Even without applied bias, thermal cycling at elevated temperatures (300–650K) can prompt crack formation owing to thermal mismatches among GaN, gate metallization, and $Si_xN_\gamma$ passivation. The thermo-mechanical strain concentrates primarily at the gate edges, symmetrically impacting the gate center, leading to structural damage on both the source and drain sides [40][41].

### 2.4.2 Time-Dependent Breakdown of the AlGaN/GaN Structure and Dielectrics

The polar nature of chemical bonds in GaN can instigate defect formation under the influence of a strong electric field, leading to the organization of these defects into a conductive percolative pathway. This results in a sudden increase in $I_G$. The degradation kinetics align with a time-dependent dielectric breakdown (TDDB) mechanism: during a gate state at a constant voltage in the off-state, the gate current initially becomes erratic, followed by a sudden surge of several orders of magnitude[42][43][44][45]. Conductive pathways manifest on the device's surface at the gate edge and can be detected using electroluminescence (EL) microscopy[45]. Direct observation of the damaged region, typically extending a few nanometers, demands meticulous sample preparation and transmission electron microscopy (TEM). If the leakage is due to a percolative chain of point defects, which are undetectable by TEM, the observation may be elusive. These time-dependent breakdown effects are characteristic of polar semiconductors like GaN and have also been witnessed in InGaN/GaN light-emitting diodes subjected to reverse bias tests[46].

The high electric field within the device places dielectrics under significant stress, making them susceptible to TDDB mechanisms. Notably, a critical point is the dielectric below the gate field-plate edge[47][48].

### 2.4.3 Electro-chemical GaN Oxidation

Under the influence of elevated temperatures and high electric fields, gate metals and contaminants can diffuse toward the semiconductor surface, particularly at the sidewall interface between the metal and passivation (typically $Si_xN_y$). Interdiffusion involving elements like Au, O, and others has been observed[49][50]. Under specific conditions (such as the presence of moisture, high temperatures, high electric fields, and device current), oxygen may react with GaN at the device surface, leading to the formation of pits and voids near gate edges. This can result in an increase in the parasitic resistance of access regions and a decrease in transconductance. Electrochemical dissolution of GaN can progressively damage the structure at the gate's drain edge, leading to the formation of pits and grooves associated with the presence of oxygen or water vapor, resulting in the formation of Ga and Al oxide[51].

A rather complex chain of electrochemical reactions, necessitating the presence of holes

generated by band-to-band tunneling, has been recognized as a potential mechanism for GaN surface oxidation. Additionally, other researchers observed the formation of an interfacial layer under the gate contact, comprising an amorphous layer of aluminum oxide formed from the expulsion of nitrogen and the consumption of aluminum from an as-formed interfacial layer composed of Al, Ga, O, and N[52]. Schottky and ohmic contacts on GaN and related compounds generally demonstrate stability at high temperatures[53]. Both Schottky and ohmic contacts can endure temperatures of up to 300°C for extended periods, although Ni has been reported to form NiO and Ni-nitrides starting at annealing temperatures as low as 200°C.

### 2.4.4 Hot Electron Effects

Enduring and reversible trapping and detrapping effects can induce substantial device drift, leading to alterations in threshold voltage and transconductance. These effects might stem from material quality, such as pre-existing deep levels on the surface, at interfaces, within the GaN buffer, or the semi-insulating substrate, or they may arise from process-induced instabilities, particularly concerning compensating species (Fe or C), contaminants like H, F, O, or defects[54]. Hot-electron effects, resulting in the generation of deep levels and electron trapping in dielectrics, surfaces, and interfaces under the gate, particularly in the gate-drain access region, may occur during off-state tests or, more frequently, during semi-on and on-state tests[55].

The term “hot electrons” refers to non-equilibrium electrons with sufficient kinetic energy to surpass potential energy barriers, being injected into buffer, barrier, or insulating layers, where they become trapped, break atomic bonds, and create interface states or activate traps, for instance, via dehydrogenation, as illustrated in Figure 2-6 [56][57][58]. Depending on experimental conditions, material properties, and device weaknesses, hot electrons may lead to parametric, gradual, permanent, or recoverable positive or negative threshold voltage shifts, and/or a reduction in transconductance.

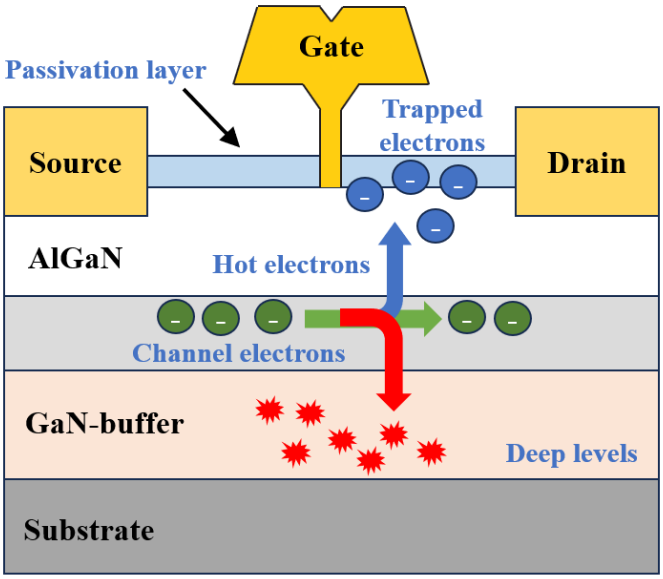



**Figure 2-5** Schematic cross-section of an AlGaN/GaN HEMT illustrating potential consequences of hot electrons: these electrons have the potential to be captured at interfaces, within the GaN buffer, on the surface, or within passivation layers[59].

In Si n-MOSFET, holes generated by impact ionization can be collected as substrate current Ib; in AlGaAs/GaAs HEMTs, impact ionization hole current induces a negative gate current Ig, which can be associated with hot-electron effects[60]. Due to the different leakage mechanisms in a GaN HEMT and the reduction of impact ionization effects because of the wide bandgap, the gate current is not indicative of hot-electron phenomena, unless the devices being studied exhibit extremely low leakage current[61].

Characterizing hot-electron effects in GaN HEMTs typically relies on the measurement of electroluminescence (EL), owing to intraband transitions of energetic electrons (Bremsstrahlung)[62]. EL exhibits a non-monotonic behavior concerning gate voltage: starting from pinch-off and increasing gate-source voltage ($V_{GS}$), EL initially increases as 2DEG density in the channel is elevated. At high $V_{GS}$, as gm saturates, EL decreases due to the electric field decrease with increasing $V_{GS}$. This characteristic can be utilized to verify if the failure mechanism is due to hot electrons by examining if, at a given drain-source voltage ($V_{DS}$), the degradation shows the same non-monotonic dependence on $V_{GS}$ as EL.

### 2.4.5 Trapping Phenomena

GaN HEMTs are known to exhibit significant trapping effects[63]. It is commonly believed that, under high voltage, surface states between the gate and the drain trap electrons that tunnel from the gate metal[64][65][66]. Additionally, hot electrons from the channel can be trapped at the surface[67]. The accumulation of these trapped electrons at the surface or within the AlGaN barrier alters the electrostatics, depleting channel carriers in the extrinsic drain, and consequently reducing the drain current[64]. In a study by Koley et al., the surface potential in the extrinsic region was measured using the Kelvin probe technique, revealing the accumulation of a negative charge on the surface when subjected to high voltage[65]. It was postulated that the trapped electrons originated from the gate and were not hot electrons from the channel, as no current flowed in the channel during their high-voltage experiment.

Although trapping at the surface or within the AlGaN barrier layer is thought to be predominant, it is also suggested that electron trapping in the GaN buffer may occur, leading to degraded device performance. Trapping in GaN HEMTs generally displays a slow nature, with a recovery time from current collapse often being long (>100 s or even a few days)[68][64][65]. This indicates that the process of detrapping trapped electrons is typically very slow. $Si_xN_y$ passivation is known to alleviate various trapping-related issues[69][70][65] by reducing trap density through the passivation of surface states and by rendering these surface states inaccessible to electrons tunneling from the gate[64]. However, the detailed mechanism of how surface passivation diminishes trapping effects remains unclear.

Efforts have been made to create dispersion-free devices using a specific cap structure[71], and sometimes even without passivation[72]. However, in most instances, surface passivation is considered crucial to alleviate trapping effects and enhance device reliability.

### 2.4.6 Reliability

Numerous researchers have extensively investigated the electrical degradation of GaN HEMTs, a notable challenge observed in GaN HEMT power applications. This degradation is evident in the reduction of drain current, transconductance, output power, $f_T$, and $f_{max}$, which has been consistently noted in various stress experiments[17][73][74]. While attempts have been made in a few studies to decipher the origins of RF output power degradation[74][75], the

prevalent approach has involved conducting DC stress tests to identify the physical degradation mechanisms.

The decrease in drain current often corresponds to an increase in drain resistance, with source resistance relatively unaffected by electrical stress[68][73]. Moreover, there is observable transconductance degradation[17][55]. Some instances have indicated a positive shift in the threshold voltage[76][73], but a unified understanding regarding the alterations in the device's threshold voltage remains elusive.

After electrical stress, increased trapping behavior has been noted in several instances[68][76]. Although reduced drain current might partially recover, it promptly reverts to its degraded state when stress resumes, signifying evidence of trap creation during stress[68]. Furthermore, gate current degradation has been reported post high voltage stress tests[73], often leading to an extensive increase in reverse gate leakage due to Schottky gate degradation. Recovery in this degradation was not observed. A significant increase in gate current can compromise RF performance, affecting parameters like PAE and gain[77].

Although Schottky characteristics can deteriorate under high voltage stress, they generally remain stable during thermal stress[77][55]. Unlike GaAs devices where gate sinking is a significant degradation mechanism, gate sinking hasn't been reported in GaN HEMTs[15][78]. Notably, apparent ohmic contact degradation hasn't been observed even after extended thermal stress[55][78] or device degradation in high voltage stress tests[79][80].

Studies have primarily focused on mechanisms affecting devices over relatively short periods since GaN HEMTs typically exhibit degradation within a few hours of high-voltage and high-temperature operation. Industry groups have reported diverse DC and RF life test results[77], yet the predicted mean time to failure (MTTF) at 300°C junction temperature varies around 150 hours. The activation energy of the MTTF typically falls between 1.05 and 2 eV, though Coffie et al. have reported a negative activation energy of -0.15 eV[81].

## 2.5 Summary

This chapter discusses the foundational aspects of GaN HEMTs and reviews previous studies concerning GaN failure mechanisms and reliability. It summarizes significant findings on the degradation observed in GaN HEMTs. Our thesis specifically concentrates on two key degradation mechanisms: hot electron effects and material defect-related trapping. We direct our attention toward minimizing these degradation mechanisms by implementing structural modifications aimed at enhancing device performance.

# Chapter 3

# Experimental setup

## 3.1 Introduction

This chapter provides an overview of the AlGaN/GaN HEMTs utilized in this study. It delves into the fabrication process and the details of the chip designed specifically for this research. Additionally, the chapter comprehensively explains the various reliability characterization methods employed throughout the study. These methods encompass interface and border trap characterization, volume trap density extraction, low-frequency noise characterizations, the pulsed *I-V* technique, and the methodology for stress characterizations.

## 3.2 Devices and fabrication processes

Throughout this study, we utilized various AlGaN/GaN HEMT structures to investigate and enhance the reliability of these devices. In Figure 3-1, you can observe the general cross-section schematics of the AlGaN/GaN HEMTs employed in our research. The wafers used in this study were generously provided by our industrial project collaborators, NTT and KANC. The epitaxial layers were grown on semi-insulating SiC/Sapphire substrates through the metal–organic-chemical-vapor-deposition (MOCVD) method. The layers were deposited in the following sequence, starting from the bottom: an AlN nucleation layer, a high-resistance GaN (or AlN) buffer layer, a GaN channel, an AlN spacer, and an $Al_xGa_{1-x}N$ barrier layer. The typical thickness of the AlGaN layer ranged from 8 to 28 nm, with an Al composition between 25% and 45%. It's worth noting that these values exhibited slight variations from one

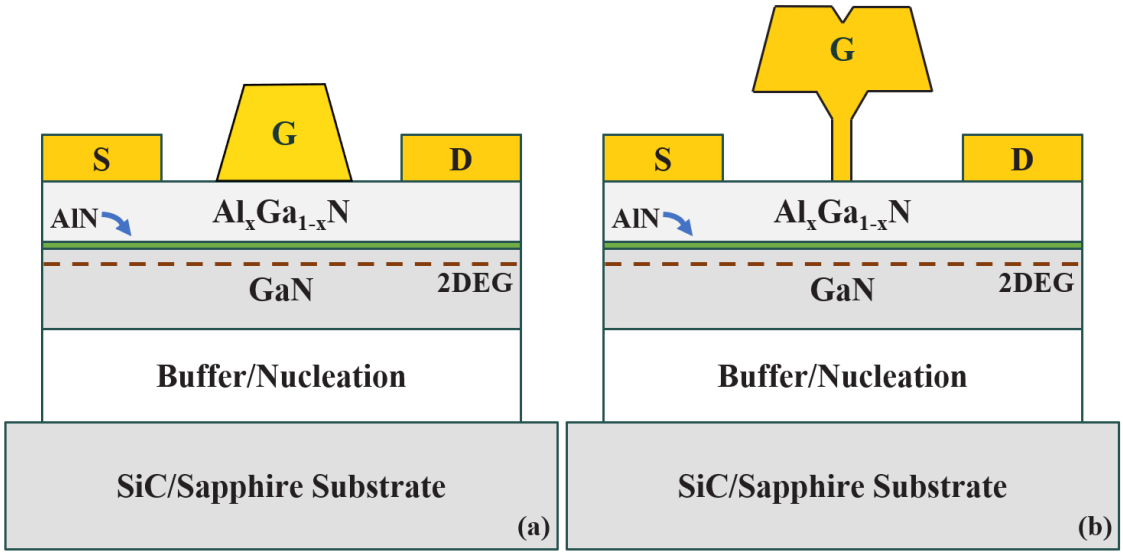



**Figure 3-1** Cross-section schematic of **(a)** Optical Trapezoidal-shaped gate. **(b)** EBL "T" shaped gate.

wafer to another. Hall measurements were conducted to determine the mobility ($\mu_{n\_Hall}$) and the sheet charge density (2DEG), yielding values ranging from 2100 to 2200 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 8 to 9 $\times 10^{12}$ $cm^{-2}$, respectively. Mesa isolation was achieved using $Cl_2$-based inductive coupled plasma (ICP) etching to isolate the individual devices. Prior to the deposition of ohmic metal, the substrates underwent a treatment involving a mixture of HCl and deionized water (1:5) for 30 seconds to eliminate any native oxide formation. To facilitate ohmic contact formation, we deposited a Ti/Al/Ni/Au (25/160/40/100 nm) alloy on the source and drain areas using an electron beam (e-beam) evaporator. Subsequently, we performed rapid thermal annealing at 830 °C in an $N_2$ ambient for 30 seconds. To determine the contact resistance ($R_C$) and sheet resistance ($R_{SH}$), we employed transmission line-method (TLM) measurements, which yielded values in the range of 0.28 to 0.5 Ω·mm and 320 to 550 Ω/□, respectively. We also deposited a Ti/Au (20/300 nm) padding layer using the e-beam evaporator to ensure robust probe contact. Finally, we deposited the gate metal, consisting of Ni/Au (20/400 nm), using the e-beam evaporator. Our research featured two types of gates: trapezoidal-shaped gate "FATFET" devices (Figure 3-1a) and "T" shaped devices (Figure 3-1b). FATFET devices had larger gate lengths ranging from 10 to 50 µm, whereas "T" shaped gate devices featured thinner channel gate lengths between 0.016 and 0.5 µm. The standard devices chosen for frequency-dependent trap analysis were the FATFET devices, whereas the majority of our reliability experiments involved devices with gate lengths of less than 0.2 µm. These standard devices had a gate width of 50 µm, and the gate-to-drain and

gate-to-source spacing was in the range of 1 to 4 µm, with the gate centered in between. A typical device with a gate width of 2 x 50 µm achieved a maximum current-gain cut-off frequency ($f_T$) of around 120 GHz and a maximum oscillation frequency ($f_{max}$) of approximately 250 GHz.

To systematically investigate reliability, we developed a dedicated reliability test chip, as illustrated in Figure 3-2. Each chip encompasses an area of approximately 63 mm² and accommodates a substantial number of the standard devices detailed previously. Most of these devices are fully processed before the via integration stage. They are arranged in close proximity, facilitating equitable comparisons during various stress experiments involving multiple devices. In addition to the standard devices, the chip also incorporates other HEMTs with distinct geometries:

- Gate fingers: 1x, 2x.
- Gate width: 5 µm, 10 µm, 20 µm, 50 µm, 2x5 µm, 2x25 µm, and 2x50 µm.
- Gate to drain distance: 1, 1.5, 2, 2.5, 4 and 6 µm.
- Source to gate distance: 1, 1.5, 2, 2.5, 4 and 6 µm.
- Butterfly-shaped FET: FET with multiple gate fingers to measure S-parameter.
- FATFET: a long gate length FET to measure capacitance.

In addition, the reliability test chip also includes different types of Transmission-Line Method (TLM):

- Standard TLMs: W=20 µm, 50 µm, 100 µm. L = 2, 3, 4, 10, 20, 30, 40 µm.
- Special TLMs: W=20 µm, 50 µm, 100 µm. L = 2, 3, 4, 10, 20, 30, 40 µm. This pattern can be utilized to measure buffer leakage current. This type of pattern also helps to get a more accurate transfer length ($L_T$) for the Wide Band Gap devices.

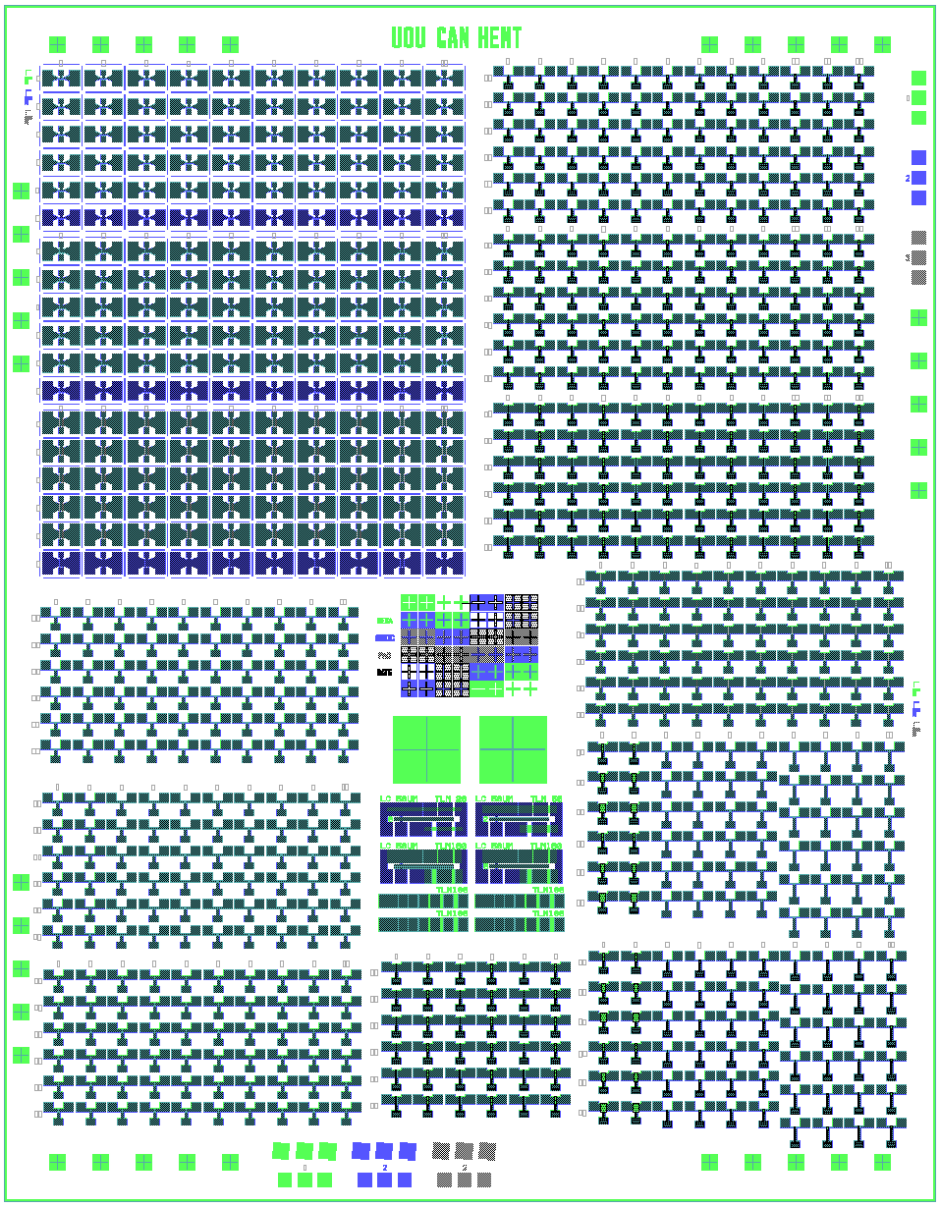



**Figure 3-2** Layout of the reliability chip used in this work.

Through the utilization of diverse HEMT and TLM variations, we are empowered to analyze the impact of various design elements on reliability. This approach allows us to pinpoint the locations of degradation, identify the primary degradation indicators, and ascertain the crucial factors influencing degradation, such as current and voltage dependencies. This test chip is seamlessly integrated into the standard process development mask. For each production wafer, multiple of these chips are meticulously fabricated. Consequently, we employ these chips from diverse wafers in the comprehensive study conducted at this stage.

### 3.3 Reliability Analysis Methods

#### 3.3.1 Interface Trap Density ($D_{it}$) Extraction

The conductance method is widely used in conventional Si MOSFET devices for the determination of interface trap density ($D_{it}$)[82][10]. In this process, the interface between the dielectric and the semiconductor is analyzed to identify trap characteristics. In this study, the conductance method was applied to the device structure. The $Al_xGa_{1-x}N$ barrier layer, characterized by its wide band gap (approximately 4 eV) and high dielectric constant (about 9.4), serves as an insulator, similar to traditional dielectric materials. The focus of the conductance method is on the extraction of the equivalent parallel conductance ($G_P$) from the measured frequency-dependent capacitance-voltage (C–V) and conductance-voltage (G–V) characteristics. In Figure 3-3, an equivalent circuit of an AlGaN/GaN HEMT in the depletion region is shown, wherein $C_{it}$, $C_S$, and $R_S$ represent the interface trap capacitance, semiconductor capacitance, and series resistance, respectively. $C_{it}$ can be expressed as $C_{it} = qD_{it}$, where '$q$' denotes the elemental charge. The conductance method was effectively utilized to extract interface traps ($D_{it}$)[82].

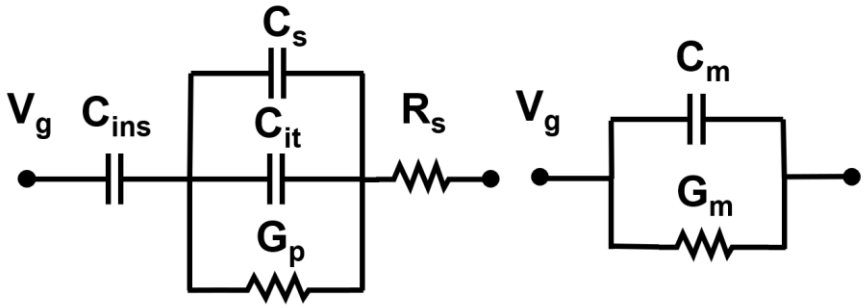



**Figure 3-3** Equivalent circuit diagram representing metal–insulator–semiconductor structure in depletion mode.

This method involves the examination of changes in trap charge states that result in system losses. Traps in closer proximity to the Fermi level ($E_F$) exhibit faster responses due to their lower response time ($\tau$). The formation of interface trap capacitance $C_{it}$ is directly influenced by electrons captured by interface traps. The evaluation of trap responses is conducted using Shockley-Read-Hall statistics, which take into account capture and emission rates[83][84][85].

$$\tau = \frac{1}{2\pi f} = \frac{1}{\omega} = \frac{e^{\left(\frac{\Delta E}{K_B T}\right)}}{\sigma \nu_{th} D_{dos}} \tag{3.1}$$

Here, $\Delta E$ represents the difference of energy between the trap level $E_T$ and the majority carrier band edge, either $E_C$ or $E_V$, $K_B$ is the Boltzmann constant and $T$ is the temperature. The cross section of traps is represented by $\sigma$, $v_{th}$ is the average thermal velocity of majority carriers, and $D_{dos}$ is the effective density of states of the majority carrier band. Figure 3-3 represents the equivalent circuit for analyzing the impedance with measured capacitance $C_m$ and measured conductance $G_m$. These measured values must be corrected for series resistance $R_s$[86]:

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{3.2}$$

Here, $C_{ma}$ and $G_{ma}$ are measured capacitance and conductance in the accumulation respectively, and $\omega$ is the angular frequency.

For the correction of capacitance and parallel equivalent conductance, we can use the following equations[82]:

$$C_c = \frac{\left(G_m^2 + \omega^2 C_m^2\right) C_m}{\left[G_m - \left(G_m^2 + \omega^2 C_m^2\right) R_s\right]^2 + \omega^2 C_m^2} \tag{3.3}$$

$$G_c = \frac{\left(G_m^2 + \omega^2 C_m^2\right)\left[G_m - \left(G_m^2 + \omega^2 C_m^2\right) R_s\right]}{\left[G_m - \left(G_m^2 + \omega^2 C_m^2\right) R_s\right]^2 + \omega^2 C_m^2} \tag{3.4}$$

The equivalent parallel conductance can be measured from the following relation[82]:

$$G_p = \frac{\omega^2 {C_{ins}}^2 G_c}{G_c^2 + \omega^2 \left(C_{ins} - C_c\right)^2} \tag{3.5}$$

Here, $C_{ins}$ is the insulator capacitance. So, $D_{it}$ can be calculated from the normalized parallel conductance peak $(G_p/\omega)_{max}$[86]:

$$D_{it} \approx \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{\max} \tag{3.6}$$

Here, A is the device area. Eq. 2-1 can be used to determine trap occupancy in the energy level where f is the frequency determined from the conductance peak $(G_p/\omega)_{max}$ [83].

### 3.3.2 Border Trap Density ($N_{bt}$) Extraction

The distributed circuit model shown in Figure 3-4 was used for the extraction of border traps[87]. It can provide information on the border trap states inside the insulator bulk with frequency-dependent C-V measurement.

This model can be represented by the following first-order differential equation[87]:

$$\frac{\partial Y}{\partial x} = -\frac{Y^2}{j\omega\varepsilon_{ins}} + \frac{q^2 N_{bt} \ln(1 + j\omega\tau)}{\tau} \tag{3.7}$$

This equation has a boundary condition of $x = 0$, $Y = j\omega CS$, while $Y$ being the total admittance. $N_{bt}$ in the above equation denotes the density of border traps in the insulator layer.

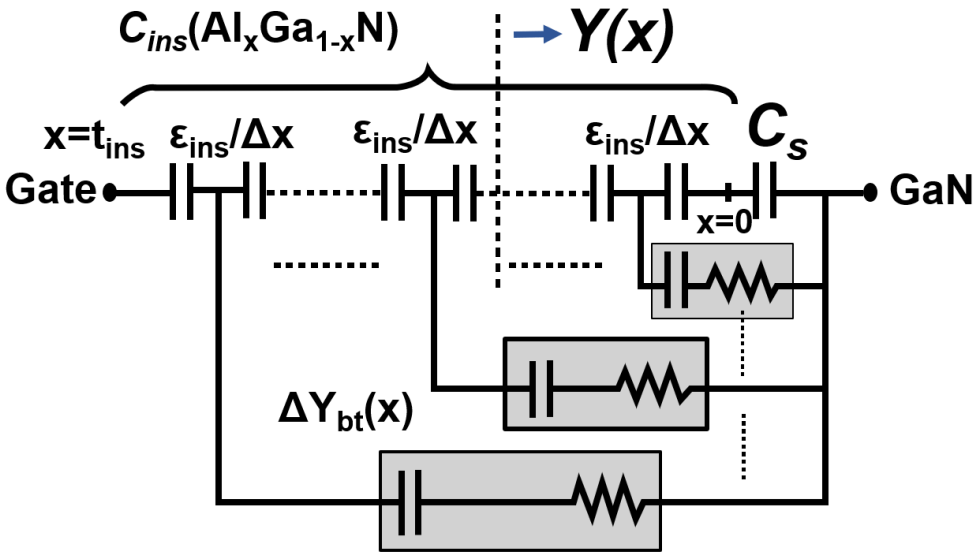



**Figure 3-4** Equivalent circuit representing distributed bulk-oxide trap model[87].

Usually, the carriers in the channel region and the border traps in the insulator layer can exchange charge through tunneling[87]. The average time ($\tau$) required for an empty trap to capture an electron can be calculated as[88],

$$\tau = \tau_{\circ} e^{2kx} \tag{3.8}$$

$$\text{Where, } k = \frac{\sqrt{2m^{*} \times E_b}}{\hbar} \tag{3.9}$$

Here, $\tau_o$ denotes the time constant of the capture and emission of a trap. $x$ denotes the distance between the interface and the trap. $m^*$ and $k$ denote the effective mass of the $Al_xGa_{1-x}N$ layer and the attenuation coefficient respectively. The barrier height between the $Al_xGa_{1-x}N$ and the GaN channel conduction band is denoted by $E_b$ and the reduced Plank's constant by $\hbar$.

$\tau_o$ can be characterized as

$$\tau_{\circ} = \left(n_s v_{th} \sigma\right)^{-1} \tag{3.10}$$

Where, $n_s$, $v_{th}$, and $\sigma$ are the electron density of the channel surface, the average thermal velocity of the electron, and the border trap cross-section area of capture/emission, respectively. Equation 3.7, can be simplified into the following equation for the total capacitance, $C_{tot}$[89],

$$C_{tot} = \frac{1}{\frac{1}{C_{ins}} + \frac{1}{2k\varepsilon_{ins}} C_2(\omega)} \tag{3.11}$$

$$C_2(\omega) = 2k\sqrt{\frac{\varepsilon_{ins}}{qN_{bt}}} \coth(B) + \ln(\omega\tau_o) - \coth^2(B) \tag{3.12}$$

$$B = a\tanh\left(\sqrt{\frac{1}{qN_{bt}\varepsilon_{ins}}C_s}\right) - \frac{1}{2k}\sqrt{\frac{qN_{bt}}{\varepsilon_{ins}}}\ln(\omega\tau_o) \tag{3.13}$$

Using $N_{bt}$ and $\tau_o$ as fitting parameters, the best-fitted curve of $C_{tot}$ with respect to frequency can be generated for the measured capacitance which will be discussed more in the results and discussion section.

The probing distance ($X_p$) of a border trap with a fixed frequency ($f$) while, $\omega\tau = 1$, can be described as[90]

$$X_p = \frac{1}{2k}\ln\frac{1}{2\pi f\tau_\circ} \tag{3.14}$$

### 3.3.3 Volume Trap Density ($N_t$) Extraction with 1/*f* noise characterization

To gain further insights into the trapping phenomena inside $Al_xGa_{1-x}N$ barrier, 1/*f* low-frequency noise (LFN) characterizations were performed from subthreshold to accumulation at a frequency range of up to $10^4$ Hz and a fixed drain bias ($V_{DS}$ = 0.1/0.5 V). All the noise measurements were performed with SRS SR570 low–noise current preamplifier, HP 35670A dynamic signal analyzer. With the LNF data, trap characterization was performed using a carrier mobility fluctuation (CMF) model as it provides accurate and reliable results in all operation regions of a transistor[91][92]]. The CMF model can be represented as the following,

$$\frac{S_{ID}}{I_D^2} = \left(\frac{G_m}{I_D}\right)^2\left(1+\alpha_{SC}\mu_{eff}C_B\frac{I_D}{G_m}\right)^2 S_{Vfb} \tag{3.15}$$

Here, $S_{ID}/I_D^2$, $\alpha_{sc}$, and $\mu_{eff}$ are the drain current noise spectral density, Coulomb scattering coefficient, and effective carrier mobility, respectively. $C_B$ is the dielectric capacitance and $S_{Vfb}$ is the flat–band voltage spectral density. Considering the tunneling process as the physical trapping mechanism into the gate dielectric, the $S_{Vfb}$ takes the form that can be defined as[91],

$$S_{Vfb} = \frac{q^2 kT \lambda N_t}{WLC_B^2 f} \tag{3.16}$$

Where $q$, $kT$, and $N_t$ are elemental charge, thermal energy, and volume trap density, respectively. λ is the attenuation distance of tunneling, which is defined as

$$\lambda = \left[ \frac{4\pi (2m^* \Phi_B)^{\frac{1}{2}}}{h} \right]^{-1} \tag{3.17}$$

Where $\Phi_B$ is the barrier height and $h$ is the planks constant[93]. A good correlation between the drain current noise level $S_{ID}/I_D^2$ and the corresponding $(G_m/I_D)^2$ over a wide drain current range can indicate that the LFN is attributed to the CMF model. The volume trap density $N_t$, can be extracted using the expression 3.16 of the flat-band voltage spectral density.

### 3.3.4 Single Short Pulse I-V characterization technique

Pulsed I–V measurements of AlGaN/GaN HEMTs offer a means to obtain "trapping-free" *I–V* characteristics, enabling the characterization of factors that may potentially contribute to the degradation of the "intrinsic" device performance. These measurements involve applying a trapezoidal or triangular $V_G$ pulse to the gate of a transistor configured as an inverter and subsequently measuring $I_D$, the drain current. The setup for this process is depicted in Figure 3-5, where the response of the drain voltage is converted to $I_D$ and graphed against the pulse bias, $V_G$, or pulse time. From the $V_D$ response, $I_D$ (in the linear regime) can be calculated as[94]

$$I_D = \frac{V_{DD}}{V_D} \left( \frac{V_{DD} - V_D}{R_L} \right) \tag{3.18}$$

In this context, $V_{DD}$ represents the drain voltage, $V_D$ corresponds to the drain response voltage, and $R_L$ signifies the load resistance, which, as detailed in this work, is set at 50 Ω. The ultrashort pulsed I–V measurements were conducted using a B1500A for the provision of DC bias and control, in conjunction with a Keysight B1530A WGFMU module.

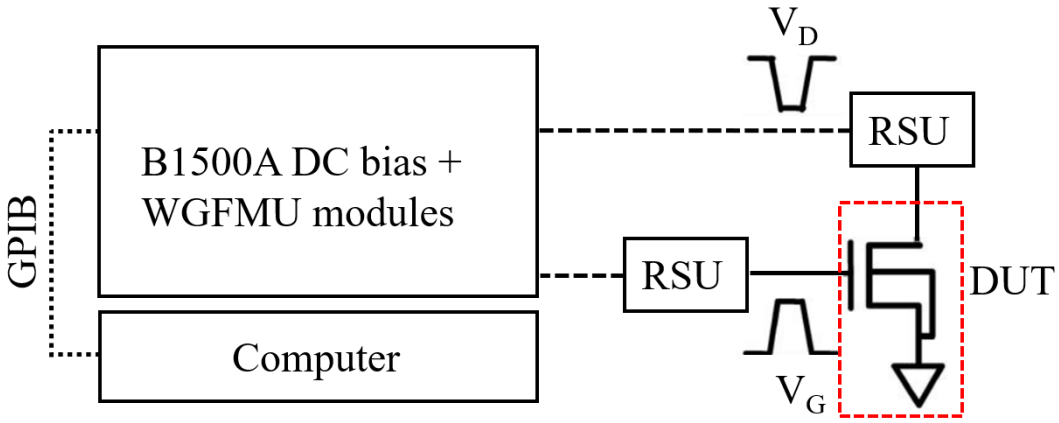



**Figure 3-5** Experimental setup for the ultrashort pulsed I–V measurement

In any pulsed I–V measurement, the total time for the pulse to rise and its width together determine the charging time, denoted as $t_p$. To prevent the occurrence of FTCE (Fast Transient Charging Effects), it is crucial that the pulse's charging time remains shorter than the onset of the trapping time, $\tau_c$. This relationship is conceptually depicted in Figure 3-6, which presents two extreme scenarios: one with ultrashort pulse times ($t_p<\tau_c$) and the other with longer pulse times. Figure 3-7 provides an example illustrating the impact of pulse rise time (charging time) on the drain current ($I_D$). The dependence on pulse rise times is reflected in the charging process, especially at higher $V_G$ values. Substantial charging during the pulse's rise time can potentially lead to an underestimation of FTCE.

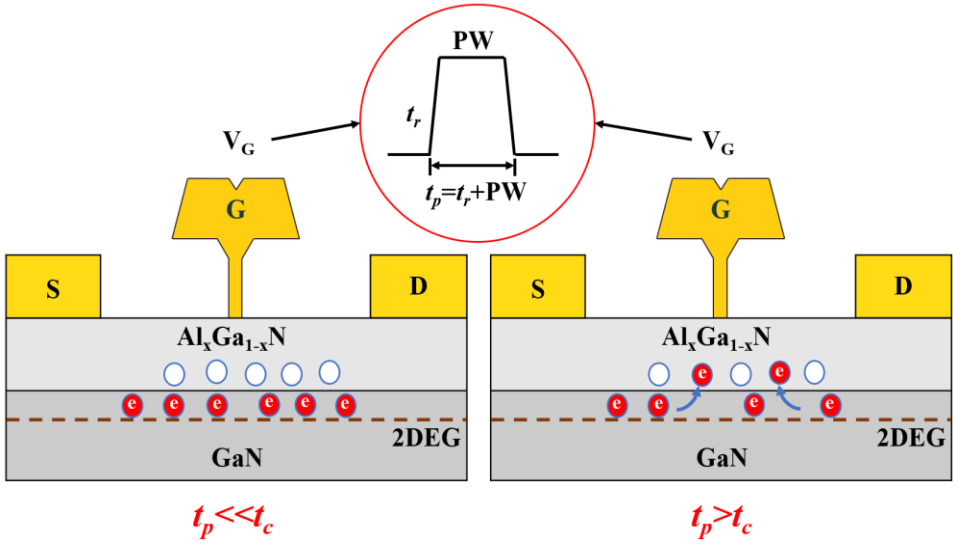



**Figure 3-6** Schematic for the electron-trapping process during the pulsed I–V measurements[95].

### 3.3.5 Stress Characterization Methodology

In detail stress characterization methods will be discussed later but in general stress procedure is explained here. Prior to subjecting the device to stress, a thorough device characterization is conducted. This comprehensive assessment covers a wide range of *I-V* characteristics, including output, transfer, gate, and subthreshold measurements. These measurements provide as-grown conditions of the device parameters. The device is then subjected to a specific stress scheme indicated in Figure 3-7. At periodic intervals, typically every 1 or 2 minutes, the stress is momentarily halted. During these breaks, a brief device characterization is performed, focusing on extracting key performance metrics such as $V_T$, $I_{Dmax}$, $G_{m\_max}$, SS, $I_G$, etc. Following the abbreviated characterization, the stress is resumed, and this stress-characterization cycle continues.

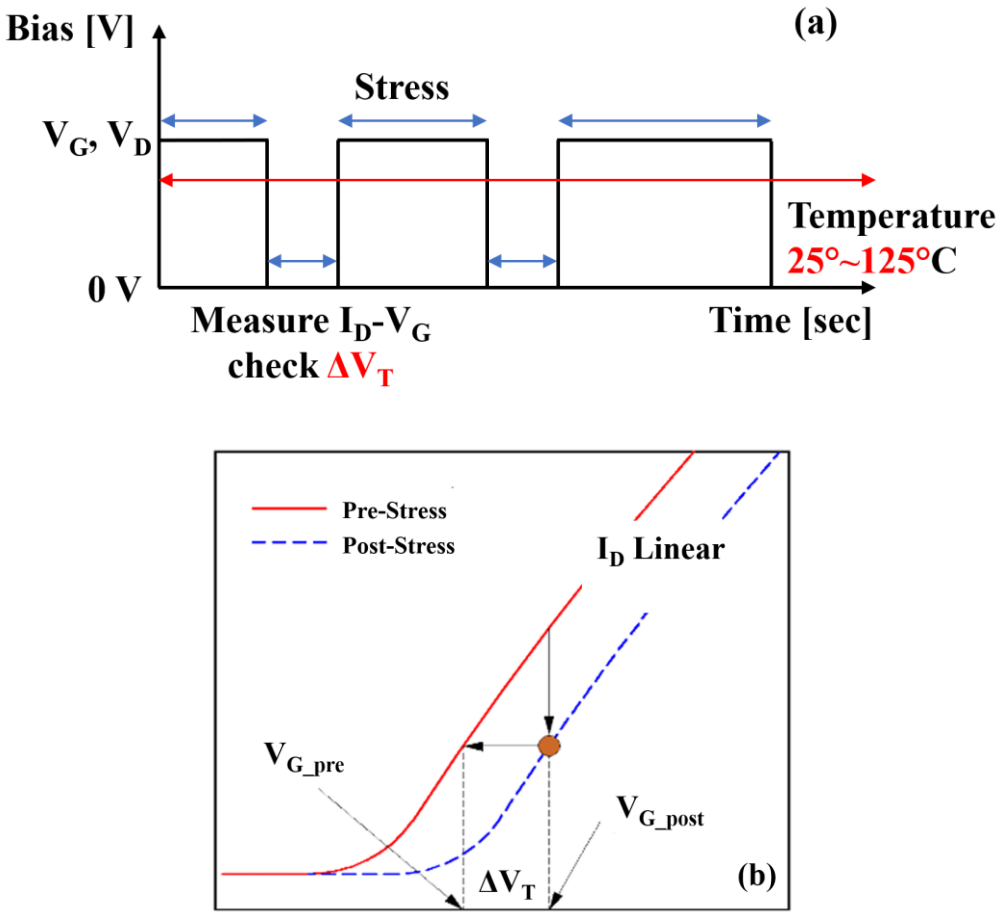



**Figure 3-7 (a)** Stress characterization Procedure used in this study **(b)** Threshold voltage shift analysis with stress characterization.

Finally, after the conclusion of the stress test or at designated points within the stress experiment, recovery phase was analyzed by repeating the same process but providing no stress bias. Instead, $V_G$ and $V_D$ biases were kept at 0 V during recovery time. Similar device characterizations were conducted to see the recovery after stress in the devices. These stress and relaxation measurements provide insight into the long-term reliability instability caused by electron trapping and detrapping in the devices.

### 3.4 Summary

In this chapter, details of AlGaN/GaN HEMT technology and the steps involved in the fabrication process were provided. We also introduced the device test chip, a crucial component in our research, and outlined the methods used for characterizing traps within the devices. Our goal was to improve the reliability of AlGaN/GaN HEMTs, and to achieve this, we harnessed various trap extraction techniques. One of the key aspects of our study involved subjecting these devices to stress experiments, a pivotal step in assessing device degradation. During these experiments, we were able to extract essential figures of merit that played a fundamental role in evaluating device performance under different stress conditions. These measures allowed us to gain valuable insights into the mechanisms of degradation within the devices.

The following chapters will dive deeper into our findings, presenting the experimental results of the reliability experiments. This will provide a comprehensive understanding of the degradation phenomena observed in these devices and the impact of various factors on their reliability.

# Chapter 4

# Interfacial Traps in AlGaN/GaN HEMTs

## 4.1 Introduction

This chapter provides an in-depth overview of the extraction of interfacial trap densities in AlGaN/GaN HEMTs. We report for the first time the use of conventional frequency-dependent C-V and G-V methods to characterize the interface trap density ($D_{it}$) between AlGaN and GaN and the deep-level/border trap density ($N_{bt}$) in the AlGaN barrier layer in a long-channel AlGaN/GaN HEMT fabricated on a SiC substrate. Typically, these frequency-dependent C-V and G-V methods are used to analyze trapping characteristics of dielectrics/oxides in a MOS structure. However, we applied these methods to our device structure because the $Al_{0.25}Ga_{0.75}N$ barrier layer has a wide band gap (approximately 4 eV) and a high dielectric constant (about 9.4), making it act like an insulator and perform similarly to a dielectric material. We mainly focused on the trap states inside the AlGaN layer, located at the interface and near the interface of the AlGaN/GaN, and tried to eliminate other probable interfacial trap contributing factors such as dielectric layers for passivation. We used the conventional frequency-dependent C–V and G–V characteristics to understand the interactions of the interface traps[82][96]. Along with these characteristics, we also investigated the deep-level/ border trap behavior in the accumulation region by examining split C–V characteristics, which are typically observed in the conventional Si MOS structure[87][97]. Although some researchers have discussed border/bulk trap extraction with threshold voltage shift profiling, discharging-based trap energy profile technique, etc., the frequency-dependent CV method for border trap density extraction for AlGaN/GaN heterostructure is not present[98][99]. We further performed validating trap characterizations to check the authenticity of our extracted results.

### 4.2 Defect sites in the AlGaN/GaN interface

In previous work, we have systematically carried out the interfacial trap analysis of AlGaN/GaN HEMTs[10]. Though AlGaN/GaN HEMTs are highly promising in high power and high-frequency applications, they suffer from reliability issues due to trapping and defect sites[100][101]. The rough interface of the AlGaN and GaN is mostly the reason for these defect sites and trapping phenomenon. Characterization of interface traps and deep-level border traps is important for improving the 2DEG carrier concentration and reducing interface roughness scattering to enhance mobility, with the eventual aim of improving device reliability and performance. Figure 4-1 shows the location of these traps in the band diagram. Interface traps are located at the interface of the AlGaN/GaN and border traps are inside the AlGaN barrier near the interface of the AlGaN/GaN. Figure 4-1 also illustrates how the tunneling of electrons occurs from the GaN channel to AlGaN layer during device operation. However, the effect of these interfacial traps is a great stimulus for the on-state act of a HEMT. Because the fermi level ($E_F$) is pinned inside the conduction band, these interfacial traps prevent the formation of sufficient carriers in the channel, which leads to reduced carrier mobility by phonon scattering and eccentricity of the threshold voltage[101][102]. These traps are also responsible for the reduction

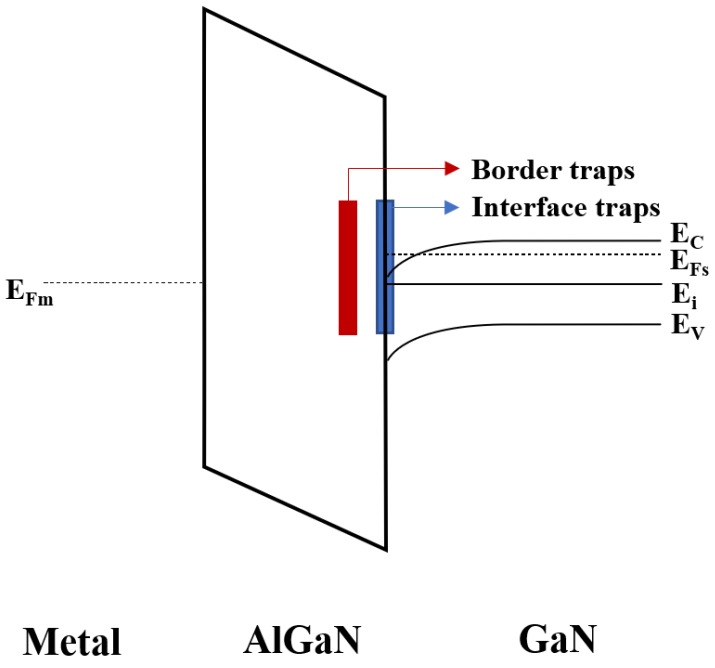



**Figure 4-1** Band diagram illustration of AlGaN/GaN HEMT showing interface and border trap sites.

of gate voltage control on the channel current, enhancing gate leakage current, a degradation of transconductance as well as for hysteresis[103][104]. The impact of interface traps is more prominent in the depletion region whereas border traps are more prominent in the accumulation region, where dispersion is always observed in the capacitance-voltage (C-V) response of the HEMTs[106]–[109]. Figure 4-2 (b) illustrates the region where the interface and border traps are

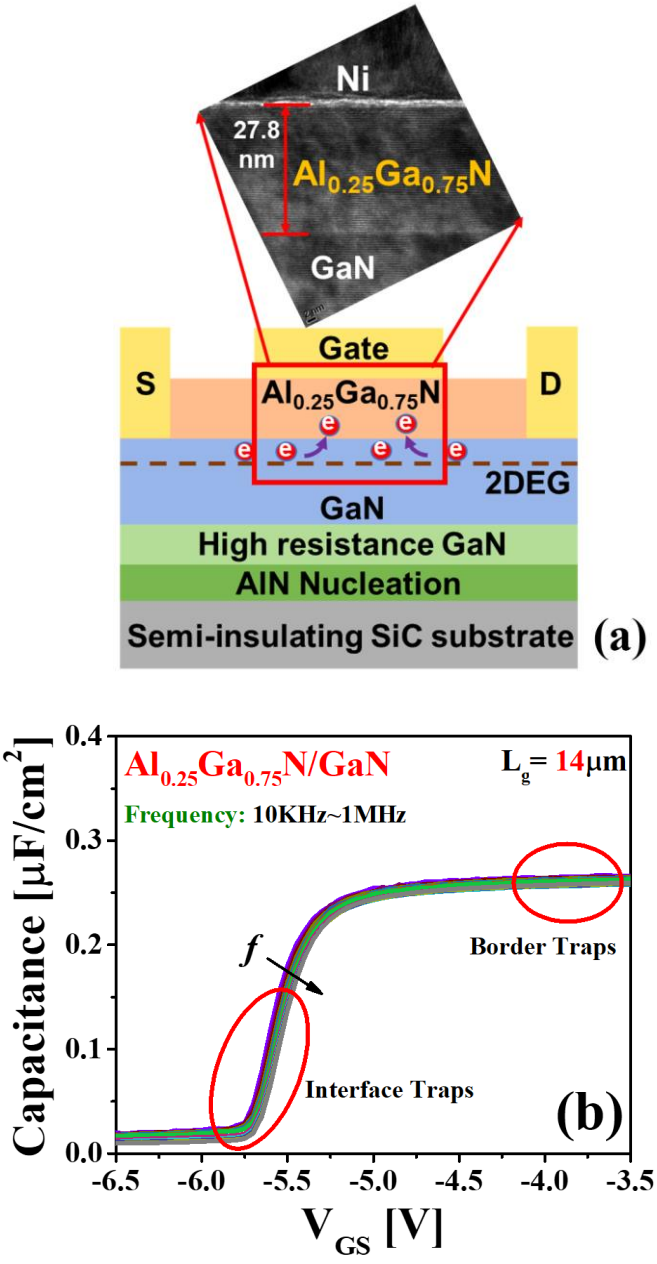



**Figure 4-2 (a)** Schematic cross-section and high-resolution TEM image of $Al_{0.25}Ga_{0.75}N$/GaN device. **(b)** Results of frequency-dependent C–V measurements showing active response region of traps.

prominent as an active trap state in capacitance-voltage (C-V) with a frequency dependency from 10 kHz to 1 MHz. The electrical behavior of border traps is quite different from that of interface traps in several ways. Firstly, the interface traps are inactive at the energy value of the accumulation region, where the frequency scattering occurs[107]. Secondly, compared with the time constant that is responsible for the interface trap's charging/discharging, the dispersion performance is less temperature-dependent because of the border traps[110].

### 4.3 Experimental details for the interfacial trap analysis

Figure 4-2 (a) illustrates the cross-sectional schematic and the transmission electron microscopy (TEM) image of the HEMT device used in this study. Epitaxial layers were grown on a semi-insulating 330 µm SiC substrate by metal–organic-chemical-vapor-deposition (MOCVD). Layers were deposited from bottom to top in the following order: an AlN nucleation layer, a 2.6 µm high-resistance GaN layer, a 150 nm GaN channel, and a 28 nm Al0.25Ga0.75N barrier layer. Hall measurements revealed the mobility ($\mu_{n\_Hall}$) and the sheet charge density (2DEG) to be 2200 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and $9 \times 10^{12}$ $cm^{-2}$, respectively. Mesa isolation was carried out with $Cl_2$-based inductively coupled plasma (ICP) etching to isolate the devices. Before ohmic metal deposition, the substrate was diluted with a mixture of HCl and deionized water (1:5) for 30 s to remove any kind of formed native oxide. To facilitate ohmic contact formation, a Si/Ti/Al/Ni/Au (1/25/160/40/100 nm) alloy was deposited on source and drain area using an electron beam (e-beam) evaporator and rapid thermal annealing at 830 °C was subsequently performed in $N_2$ ambient for 30 s. The contact resistance ($R_C$) and sheet resistance ($R_{SH}$) were extracted by transmission line-method (TLM) measurements to be 1.2 Ω·mm and 320 Ω/□ respectively. A Ti/Au (20/300 nm) padding layer was deposited using the E-beam evaporator to achieve strong probe contact. Finally, gate metal consisting of Ni/Au (20/400 nm) was also deposited using e-beam evaporator. The gate length ($L_g$), gate width ($W_g$), and source-to-drain distance ($L_{sd}$) of the fabricated devices were 14, 50, and 18 µm, respectively. All the devices had the same source-to-gate ($L_{sg}$) distance and gate-to-source distance ($L_{gd}$) of 2 µm. From the high-resolution TEM image shown in Fig. 1a, the well-deposited $Al_{0.25}GaN_{0.75}N$/GaN interface can be observed. The thickness of $Al_{0.25}GaN_{0.75}N$ was well around 28 nm (27.8 nm) and formed a good interface with the GaN channel layer.

### 4.4 Extraction of interface trap densities ($D_{it}$)

Figure 4-2 (b) shows the results of the frequency-dependent *C–V* measurements of the $Al_{0.25}GaN_{0.75}N$/GaN HEMT where frequency dispersion is evident. Frequency dispersion can be caused by various reasons. Some of the main causes of frequency dispersion during C–V measurement are parasitic effect, lossy interfacial layer, surface roughness, and quantum mechanical confinement etc[111]. Among them, the most influential reason is the lossy interfacial layer of AlGaN/GaN. The trap states in the AlGaN layer are mostly the reason behind the dispersion. The frequency dispersion in the depletion region indicates that this region is the dominant region for interface traps, whereas the dispersion in the accumulation region indicates the dominant region of the border traps. We used the Nextnano simulation tool (one-dimensional Poisson–Schrodinger solver) to compare the measured and simulated capacitance with respect to

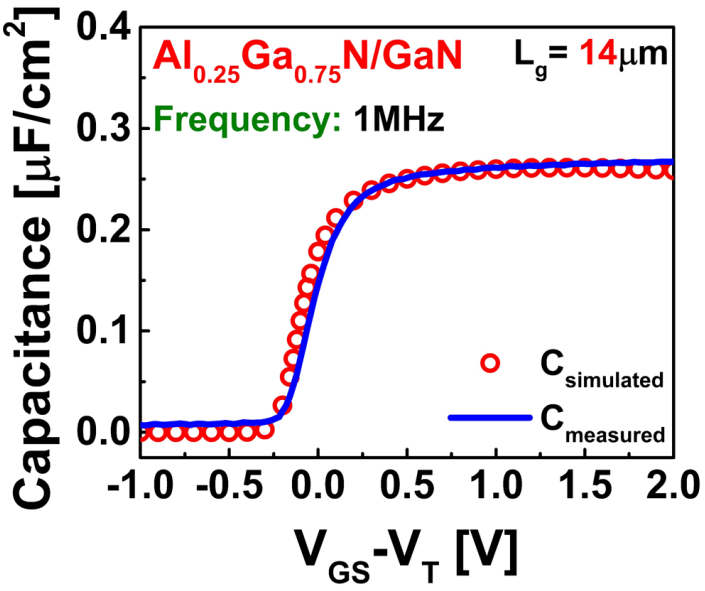



**Figure 4-3** Comparison between measured and simulated C–V characteristics.

a constant gate overdrive ($V_{GS} - V_T$), as shown in Figure 4-3. It is evident that both the measured and the simulated C–V curves are similar which indicates a lower leakage current effect on the measured data. Thus, the AlGaN layer can be treated as an insulator owing to its high dielectric constant, similar to the MIS/MOS structure.

Figure 4-4 (a) & (b) show the band diagrams (determined via simulation) in the depletion and accumulation regions, respectively. In the depletion region, the interface traps above the Fermi level $E_F$ are mostly active; this causes the capture and emission of the carriers in the

channel region. In the accumulation region, where $E_F$ penetrates the conduction band $E_C$, the electrons on the surface are captured and emitted by the border traps via tunneling. A Keysight B1500A semiconductor device analyzer and an Agilent 4384A precision LCR meter were used for all DC measurements.

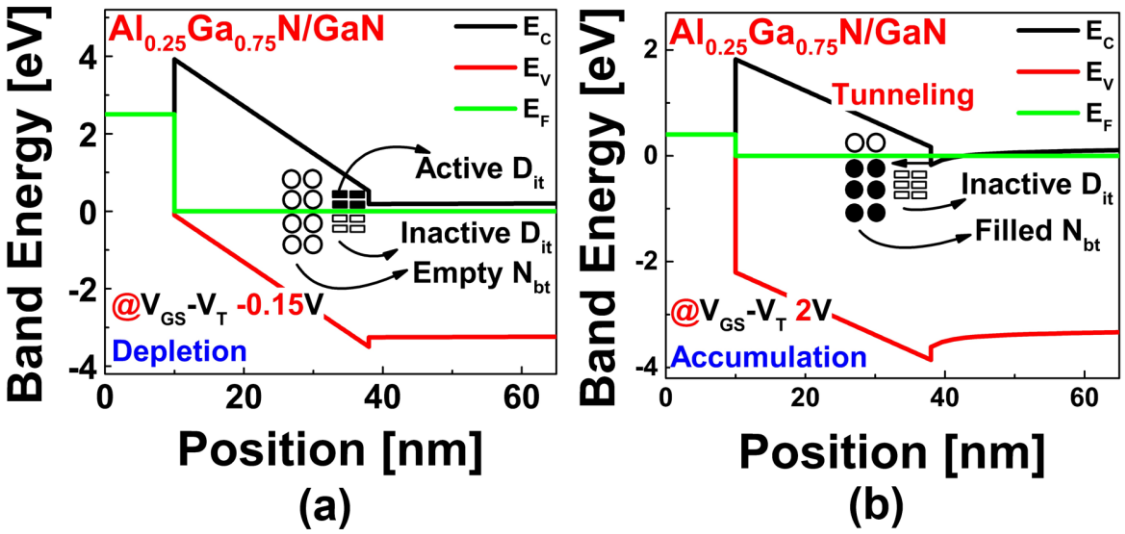



**Figure 4-4** Simulated band diagram showing trap behavior **(a)** in depletion and **(b)** in accumulation.

The insulator capacitance was determined by the following equation:

$$C_{ins} = \frac{\varepsilon_{\circ}\varepsilon_{ins}}{t_{ins}} \tag{4.1}$$

Here, $\varepsilon_o$ is the permittivity of free space and $\varepsilon_{ins}$ is the relative permittivity of the $Al_{0.25}Ga_{0.75}N$ layer. As it is known from the literature, the value of $\varepsilon_{ins}$ as calculated from $\varepsilon = -0.5x + 9.5$—where x denotes the Al content of the $Al_xGa_{1-x}N$ layer—for x = 25% is around 9.375[29,30. The tensor components of AlN and GaN's {0001} relative permittivity are linearly interpolated to obtain the relation. The parallel equivalent conductance $G_p$ was calculated using Eq. 3.5 with correction of the measured capacitance and conductance for the series resistance. Figure 4-5 shows a plot of the parallel conductance $G_p/\omega$ versus the angular frequency $\omega$. $D_{it}$ was measured from the $(G_p/\omega)_{max}$ peak, using Eq. 3.6; The extracted value of $D_{it}$ using the conductance method was in the range of $2.5 \times 10^{12}$ $cm^{-2}\cdot eV^{-1}$ to $7.1 \times 10^{12}$ $cm^{-2}\cdot eV^{-1}$ which is

well within the range of $10^{11}$–$10^{14}$ $cm^{-2}$ $eV^{-1}$ for S-HEMT and MOS-HEMT from literature[112][113][114].

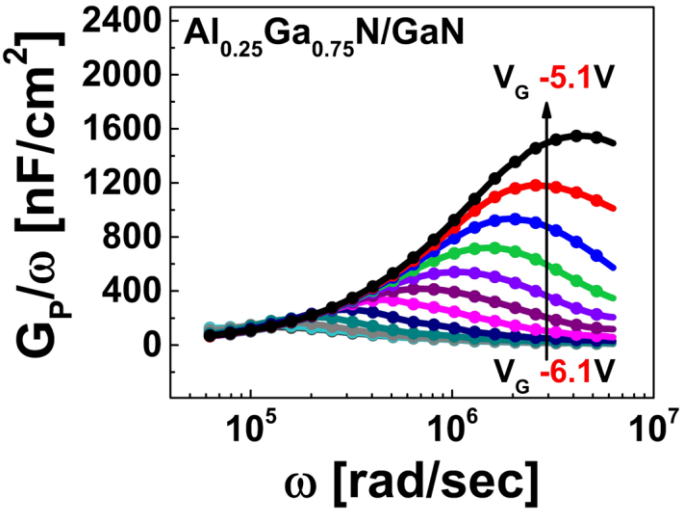



**Figure 4-5** Equivalent parallel conductance ($G_P/\omega$) with respect to the frequency at different gate bias points.

Figure 4-6 shows the active $D_{it}$ with respect to the trap energy ($\Delta E$), which was determined from Eq. 3.1. For this calculation, the frequency corresponding to $(G_p/\omega)_{max}$ was considered. At room temperature (300 K), the average thermal velocity $v_{th}$ and the effective density of states ($D_{dos}$) of the GaN material were considered to be 2.6 × $10^7$ $cm{\cdot}s^{-1}$ and 1.2 × $10^{18}$ $cm^{-3}$, respectively[114]. The value of the capture cross-section $\sigma$ was assumed to be 3.4 × $10^{-15}$$cm^2$ from the literature[115].

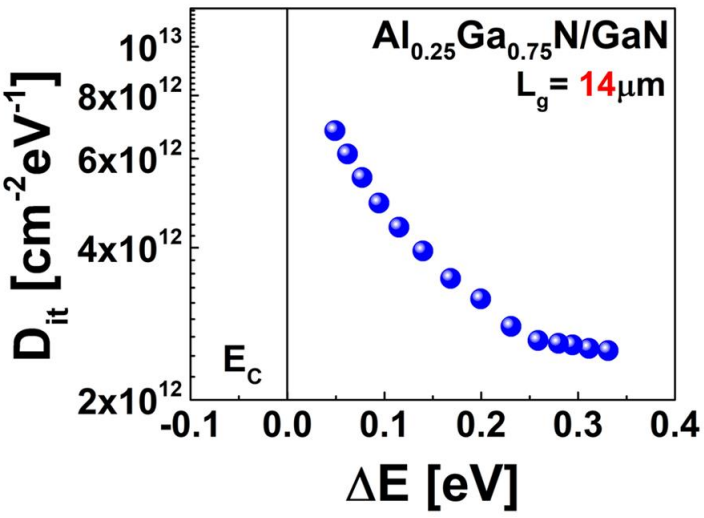



**Figure 4-6** Distribution of interface traps as a function of band energy state.

### 4.5 Extraction of border trap densities ($N_{bt}$)

We used the parameters in Table 4-1 to extract the border trap density $N_{bt}$. For the calculation of the attenuation coefficient, the effective mass of $Al_{0.25}Ga_{0.75}N$ was considered to be $0.19m_o$ (where $m_o$ denotes the electron mass at rest)[116]. The semiconductor capacitance $C_S$ was estimated via Nextnano simulation at an accumulation gate bias of −3.5 V, which was the primary $N_{bt}$ extraction voltage considered in this study. From Eq. 3.7, the best-fitted capacitance curves were obtained at −3.5 V under consideration of $N_{bt}$ and $\tau_o$ as variable fitting parameters. The best-fitted curve was obtained at $N_{bt} = 1.5 \times 10^{19}$ $cm^{-3}\cdot eV^{-1}$ and $\tau_o = 1 \times 10^{-12}$ s, as shown in Figure 4-7. Here, $C_M$ denotes the capacitances measured at various applied frequencies at −3.5 V and $C_{tot}$ represents the fitted curve. The spatial distribution of $N_{bt}$ as a function of both the applied $V_{GS}$ and the probing distance into the $Al_{0.25}Ga_{0.75}N$ layer from the $Al_{0.25}Ga_{0.75}N$/GaN interface is shown in Fig. 4-8. The $N_{bt}$ values were extracted at various applied voltages at a particular applied frequency. The probing depth into the $Al_{0.25}Ga_{0.75}N$ layer from the interface was calculated by Eq. 3.14 using different $\tau_o$ values associated with the $N_{bt}$ values. Because the border traps exhibit more dominant characteristics at lower frequencies, we employed a low frequency of 10 kHz to extract the probing depth. With an increase in $V_{GS}$, the Fermi level $E_F$ tended to penetrate to a greater depth into the conduction band $E_C$. As a result, more electrons tended to tunnel into the deep-level traps. As all parameters except $\tau_o$ were fixed, $\tau_o$ showed an inverse relation with the probing depth.

**Table 4-1** Parameters used and extracted values of $D_{it}$ and $N_{bt}$

| Parameter | Value |
|---|---|
| $t_{ins}$ [nm] | 28 |
| $\varepsilon_{ins}$ | 9.375 |
| $m^*$ [$m_o$] | 0.19 |
| $E_b$ [eV] | 0.8 |
| $k$ [$nm^{-1}$] | 1.99 |
| $C_S$ [$\mu F\cdot cm^{-2}$] | 0.27 |
| $\tau_o$ [s] | $1 \times 10^{-12}$ |
| $D_{it}$ [$cm^{-2}\cdot eV^{-1}$] | $2.5 \times 10^{12}$ |
| $N_{bt}$ [$cm^{-3}\cdot eV^{-1}$] | $1.5 \times 10^{19}$ |
| $N_t$ [$cm^{-3}\cdot eV^{-1}$] | $1.3 \times 10^{19}$ |

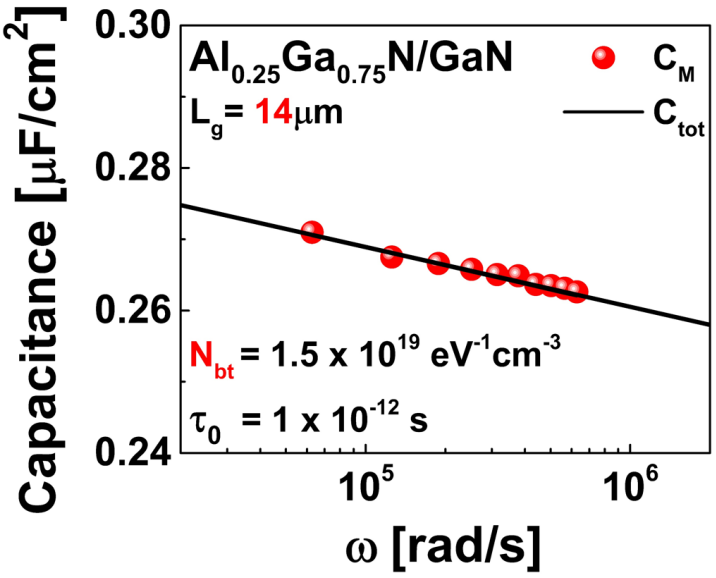



**Figure 4-7** Fitting curves generated using a distributed circuit model at $V_{GS}$ = − 3.5 V.

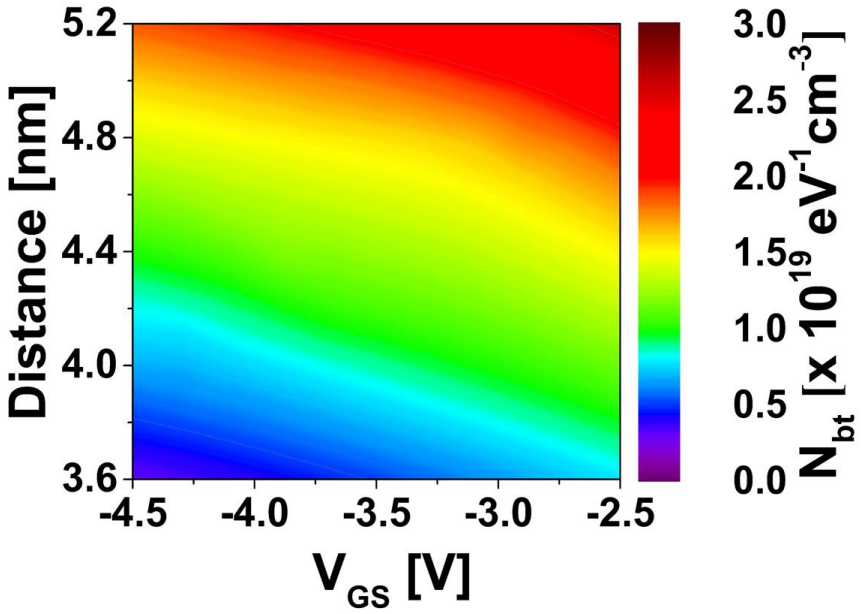



**Figure 4-8** Contour mapping of border trap distribution in $Al_{0.25}Ga_{0.75}N$ layer from $Al_{0.25}Ga_{0.75}N$/GaN interface.

### 4.6 Reliability Validation of the extracted $D_{it}$ & $N_{bt}$

Previously, the $D_{it}$ & $N_{bt}$ of the dielectric/oxide layers of the transistors were extracted via frequency-dependent C-V and G-V method. So, our approach of using these methods to extract $D_{it}$ & $N_{bt}$ of the AlGaN/GaN interface is relatively new and need validation via external methods. The reliability of the extracted value of $D_{it}$ was determined via a theoretical calculation of the subthreshold swing (SS) using the following equation[117]:

$$SS = \frac{kT}{q}\ln 10.\left(1+\frac{qD_{it}}{C_{ins}}\right) \tag{4.2}$$

The value of the SS calculated from the lowest extracted $D_{it}$ was around 143 mV·dec$^{-1}$, whereas the value determined by the basic $I$–$V$ measurement was found to be 142 mV·dec$^{-1}$ (Figure 4-9). This similarity of the measured and calculated values confirms the reliability of the extracted value of $D_{it}$.

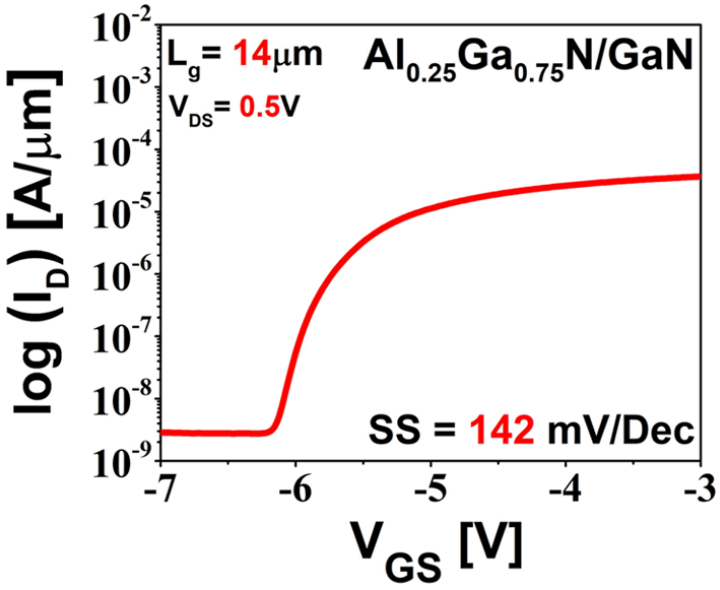



**Figure 4-9** Transfer characteristics (*log* ($I_D$)–$V_{GS}$) showing SS of device.

1/f noise measurements were performed by varying the gate voltage $V_{GS}$ and fixing the drain bias $V_{DS}$ at 0.5 V. Figure 4-10 (a) shows the normalized $S_{ID}/I_D^2$ (drain current noise spectral density) with respect to frequency up to $10^4$ Hz under varying $V_{GS}$ from the linear region. It is evident that as $V_{GS}$ increased, and the device transitioned from weak inversion to strong inversion,

the noise level ($S_{ID}/I_D^2$) decreased. Plotting of the normalized $S_{ID}/I_D^2$ as a function of $I_D$ (drain current) provided results that were more explanatory. Figure 4-10 (b) shows a plot of the normalized $S_{ID}/I_D^2$ (blue spheres) as a function of $I_D$ at a frequency of 10 Hz. The channel carrier trapping phenomenon of the gate dielectric can be explained using the carrier mobility fluctuation (CMF) model by the equations 3.15 and 3.16[92][118][119].

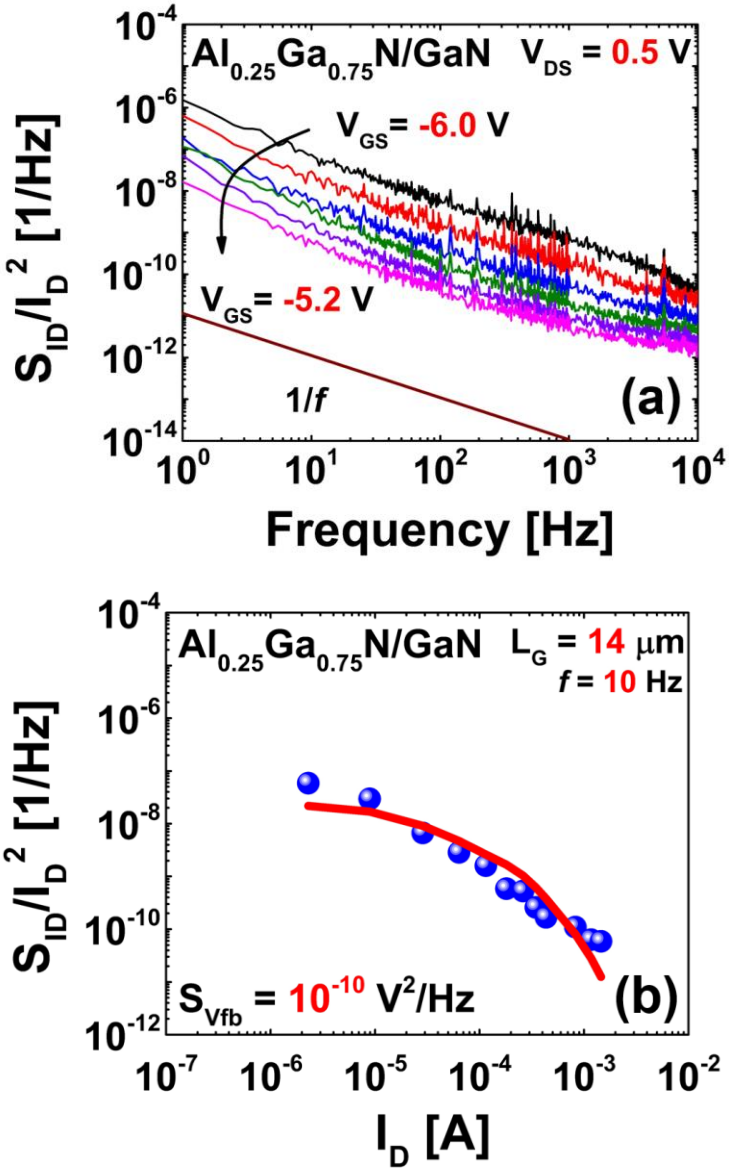



**Figure 4-10 (a)** Noise spectral density ($S_{ID}/I_D^2$) with respect to frequency at various gate bias ($V_{GS}$) points. **(b)** Noise spectral density ($S_{ID}/I_D^2$) and $(g_m/I_D)^2$ as functions of drain current $I_D$.

According to the CMF model, the terms $S_{ID}/I_D^2$ and $(g_m/I_D)^2$ vary in similar ranges with the drain current or gate voltage. From Fig. 4-9.b, it is evident that both $S_{ID}/I_D^2$ (blue spheres) and $(g_m/I_D)^2$ (red line) vary similarly over several decades under varying $I_D$. The $S_{Vfb}$ value was calculated to be $10^{-10}V^2 \cdot Hz^{-1}$ from Eq. 2.15. Using Eq. 2.16, we then calculated the border trap density (Volume Trap Density) $N_t$ to be around $1.3 \times 10^{19}$ $cm^{-3} \cdot eV^{-1}$; this value is of a similar level to the values of the border trap density $N_{bt}$ extracted from the distributed circuit model and well comparable to the data from literature of $10^{18}$–$10^{22}$ $cm^{-3}$ $eV^{-1}$[120][121][122].

## 4.7 Summary

Unlike previous studies, which focused mainly on the insulator/AlGaN interface for trap extraction, we attempted to investigate the AlGaN/GaN interface for this purpose. We used modified versions of conventional MOS trap extraction methods to extract the interface trap density $D_{it}$ and border trap density $N_{bt}$ of the $Al_{0.25}Ga_{0.75}N$/GaN interface. We performed the extractions by considering the $Al_{0.25}Ga_{0.75}N$ layer to be comparable to the insulator of the MOS structure on account of the relatively high dielectric constant of the former. We further validated the values of $D_{it}$ & $N_{bt}$ that we extracted by comparing them with theoretical and experimental calculations, as well as references from the literature. In the following chapter, in-depth reliability assessment of the $Al_xGa_{1-x}N$/GaN HEMTs [x= 0.25, 0.45] with a variation in the Al composition in presented and device degradation phenomena are discussed.

# Chapter 5

# Impact of various Al compositions in Reliability Assessment of $Al_xGa_{1-x}N$/GaN HEMTs

## 5.1 Introduction

In this chapter, we present a detailed analysis of trapping characteristics at the $Al_xGa_{1-x}N$/GaN interface of $Al_xGa_{1-x}N$/GaN high electron mobility transistors (HEMTs) with reliability assessments, demonstrating how the composition of the Al in the $Al_xGa_{1-x}N$ barrier impacts the performance of the device. Reliability instability assessment in two different $Al_xGa_{1-x}N$/GaN HEMTs [x = 0.25, 0.45] using a single-pulse $I_D$-$V_D$ characterization technique revealed higher drain-current degradation ($\Delta I_D$) with pulse time for $Al_{0.45}Ga_{0.55}N$/GaN devices which correlates to the fast-transient charge-trapping in the defect sites near the interface of $Al_xGa_{1-x}N$/GaN. Constant voltage stress (CVS) measurement was used to analyze the charge-trapping phenomena of the channel carriers for long-term reliability testing. $Al_{0.45}Ga_{0.55}N$/GaN devices exhibited higher threshold voltage shifting ($\Delta V_T$) caused by stress electric fields, verifying the interfacial deterioration phenomenon. Defect sites near the interface of the AlGaN barrier responded to the stress electric fields and captured channel electrons—resulting in these charging effects that could be partially reversed using recovery voltages. Conversely, the $Al_{0.25}Ga_{0.75}N$/GaN device exhibited a substantial 35% reduction in interface trap density ($D_{it}$) and an impressive 73% decrease in border trap density ($N_{bt}$), solidifying its reduced trapping behavior compared to $Al_{0.45}Ga_{0.55}N$/GaN due to the rougher barrier/channel interface of the latter device. Lastly, quantitative extraction of volume trap density ($N_t$) using 1/$f$ low-frequency noise characterizations unveiled a 40% reduced $N_t$ for $Al_{0.25}Ga_{0.75}N$/GaN device, further verifying the higher trapping phenomena in the $Al_{0.45}Ga_{0.55}N$ barrier caused by the rougher $Al_{0.45}Ga_{0.55}N$/GaN interface.

### 5.2 Electron Trapping phenomenon during device operation

The fabrication process of the $Al_xGa_{1-x}N$/GaN HEMTs used in this analysis is similar to the process described in section 4.3. We utilized two distinct Al compositions of 25% & 45% for this analysis. Figure 5-1 shows the 1-D simulation of the conduction band edge ($E_c$) and carrier density ($n_o$) of the samples used in this study. Though increased Al content in $Al_{0.45}Ga_{0.55}N$/GaN improves the carrier density in the channel, the charge centroid moves closer to the $Al_xGa_{1-x}N$ barrier. The displacement of the channel carrier centroid towards the barrier layer enhances quantization effects, leading to increased trapping probability for electrons in the $Al_xGa_{1-x}N$ barrier[123].

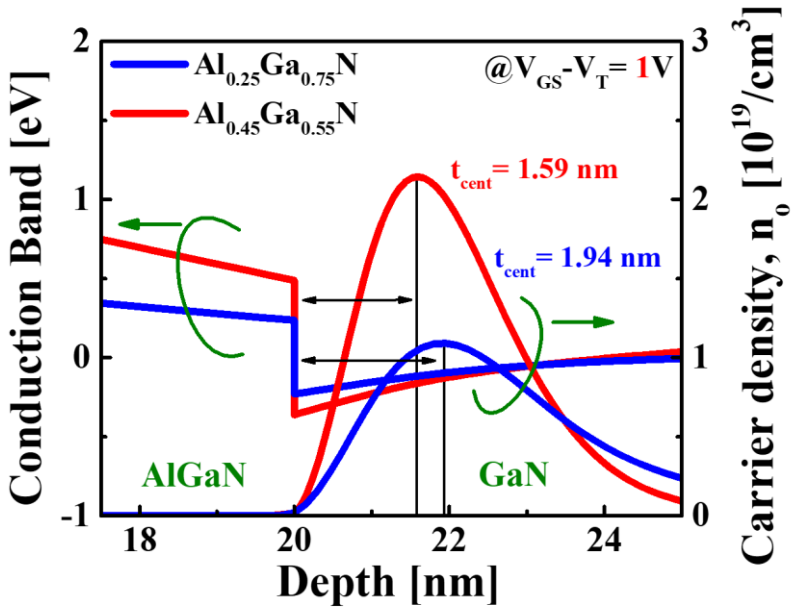



**Figure 5-1** 1-D band ($E_c$) simulation of the $Al_xGa_{1-x}N$/GaN HEMTs including the carrier density profiles ($n_o$).

Figure 5-2 (a) shows an explanatory illustration of the trapping behaviors exhibited by channel carriers. The tunneling probability of the channel electrons through the barrier increases exponentially with the increased Al composition as the tunneling distance ($d_1>d_2$) reduces[124]. This reduction in the barrier thickness (tunneling distances) can render the devices more vulnerable to hot carrier degradation, as carriers have to tunnel a shorter distance to transfer to surface states.

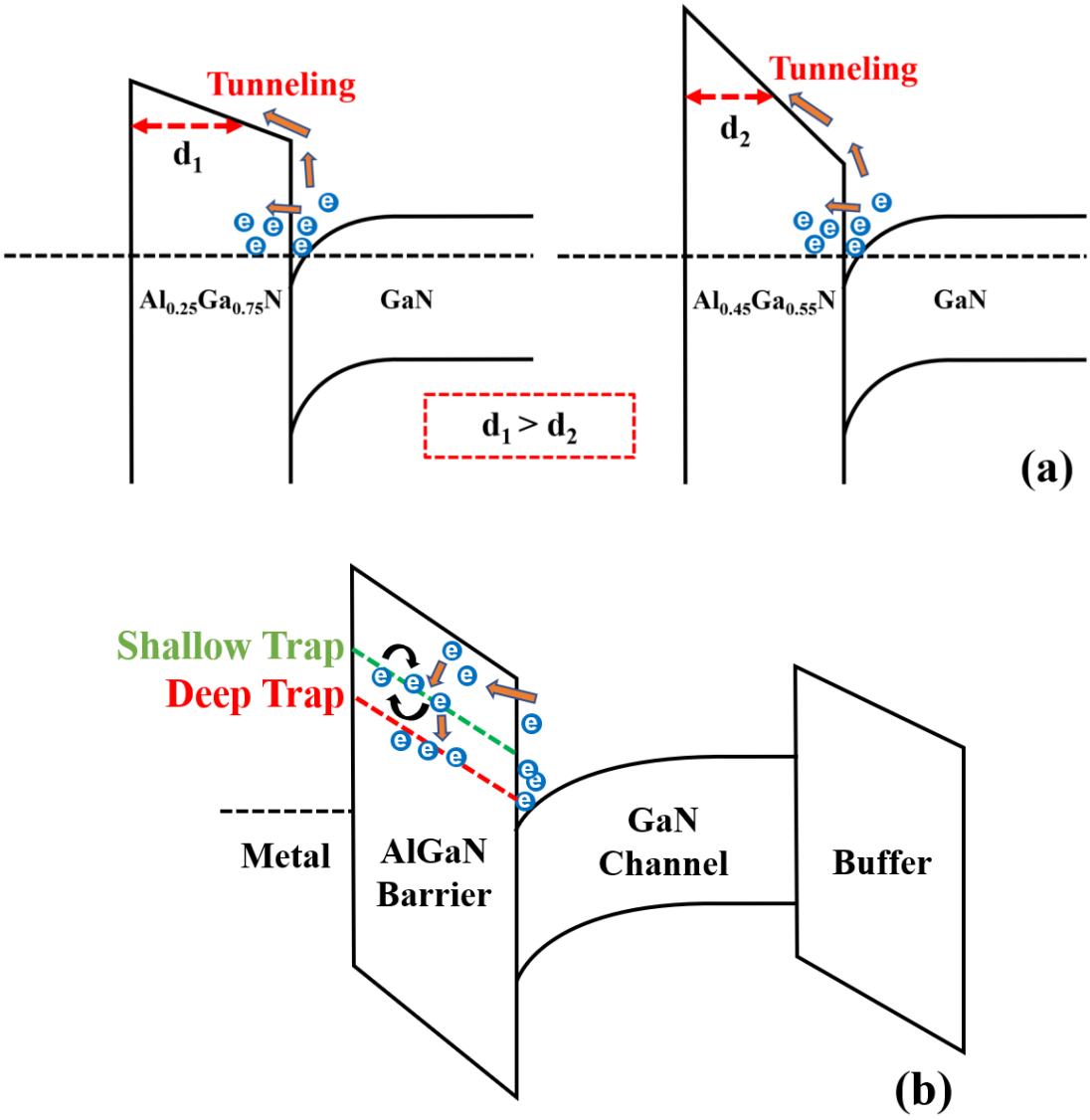



**Figure 5-2** (a) Illustration of the trapping behavior of channel electrons with varying Al composition[124] (b) Schematic of the band diagram of $Al_xGa_{1-x}N$/GaN HEMTs defining the "Shallow" and "Deep" trap states that capture tunneling channel carriers.

The defect sites in the AlGaN barrier layer and the interface $Al_xGa_{1-x}N$/GaN are the predominant cause of the transient-charging effects[125][126]. The transient-charging effects follow two different processes such as fast and slow transient charging. Channel carriers are easily injected into shallow defects (fast-transient charging) in the $Al_xGa_{1-x}N$ barrier layer and the interface of $Al_xGa_{1-x}N$/GaN. Then, trapped charges in the shallow trap site follow thermally activated electron migration via trap-to-trap conduction (slow transient charging) (figure 5-2 (b)). The fast-transient-charging effect is responsible for mobility degradation and threshold voltage

($V_T$) instability in AlGaN/GaN HEMTs, while the slow transient charging causes long-time stress $V_T$ instability. All of these are major concerns for implementing GaN-based HEMTs in future applications. Improving the reliability instability of $Al_xGa_{1-x}N$/GaN HEMTs requires thoroughly analyzing the trapping effects because the channel carriers can easily tunnel into the pre-existing defect sites in the $Al_xGa_{1-x}N$ barrier layer and the interface $Al_xGa_{1-x}N$/GaN.

### 5.3 Charge-Trapping Analysis with Pulsed I-V

Figure 5-3 (a) shows the DC transfer characteristics comparison of the devices with respect to the gate overdrive voltage ($V_{GS}$-$V_T$). Although the device characteristics are quite similar in DC measurements, the Al = 25% sample showed slightly higher drain current $I_D$ (at high $V_{GS}$-$V_T$) and transconductance $G_m$. Figure 5-3 (b) illustrates single-pulse $I_D$-$V_D$ characteristics with different Al compositions in the barrier layer. The output characteristics of a single-pulse $I_D$-$V_D$ technique with the rise ($t_r$) and fall time ($t_f$) of 50ns were measured with a $V_D$ sweep. Rise and fall times were kept small to achieve trap-free $I_D$-$V_D$ characteristics[95]. A short pulse width of the gate and drain was applied during the measurement, reducing fast-transient trapping/de-trapping effects.

A significant reduction in the drain current ($\Delta I_D$) is observed during the fall-down trace for the Al = 45% sample compared with the Al = 25% sample, related to the filling of the resonant traps during the rise time and pulse width through the fast-transient charging process. DC measurements cause a significant degradation because of higher integration time (~5 ms)[127][123][128].

Figure 5-3 (c) depicts the fast degradation in the drain-current with respect to time when the gate pulse is $V_{GS}$-$V_T$ = 2V and drain bias is $V_{DS}$ = 5V, corresponding to the pulsed $I_D$-$V_D$ characteristics. Channel carriers are trapped in the trap states near the interface of the $Al_xGa_{1-x}N$ barrier layer and the interface $Al_xGa_{1-x}N$/GaN[123][124]. $I_D$ degradation for $Al_{0.25}Ga_{0.75}N$/GaN device during 500ns pulse width is ~20 mA/mm, while $Al_{0.45}Ga_{0.55}N$/GaN device illustrates $I_D$ degradation in ~67 mA/mm. A significantly higher $I_D$ degradation for the Al = 45% sample corresponds to a rougher interface between the barrier and GaN channel caused by higher lattice mismatching.

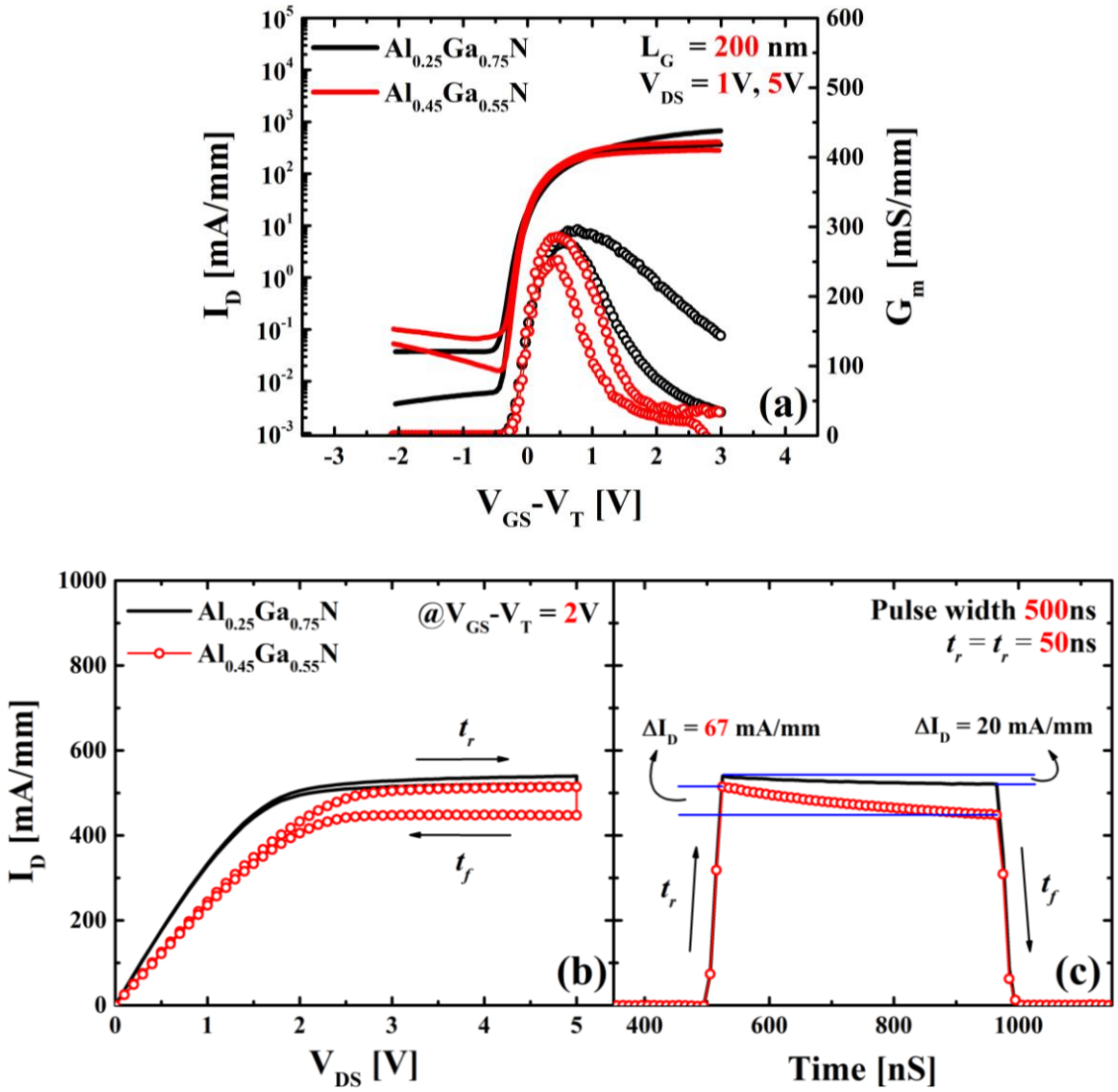


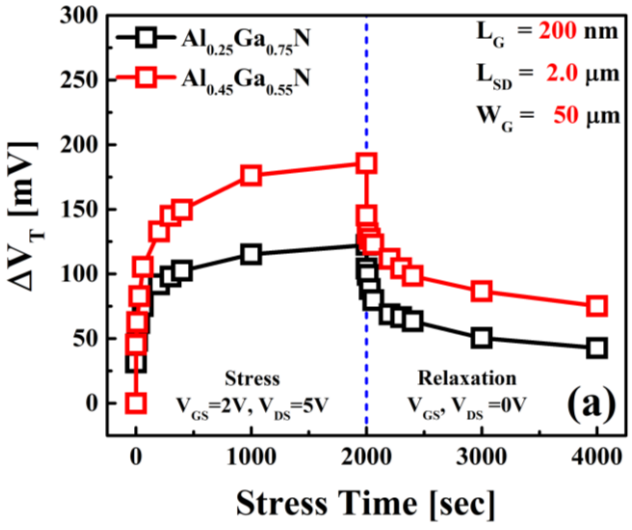

**Figure 5-3 (a)** DC transfer characteristics of the samples at $V_{DS}$ = 1, 5V with respect to the gate overdrive voltage ($V_{GS}$–$V_T$). **(b)** A single-pulse $I_D$–$V_D$ characteristics of AlGaN/GaN HEMTs with different Al compositions. **(c)** Rapid deterioration of the drain current over time when a maximum pulse is applied to both gate and drain, which is consistent with the pulsed $I_D$–$V_D$ sweep.

Drain-current degradation with respect to pulsed time is related to charge-trapping in the defect sites, which can be explained by the model of charging processes[129]. Channel carriers can be tunneled into the shallow defect sites in the AlGaN barrier layer and can occur to thermally activated electron migration between the defect sites with temperature dependency. The location

of these defect sites is below the conduction band, as illustrated in Figure 5-2 (b). Because of the extremely low trap energy of these shallow traps and the high density of states (DOE) from the GaN conduction band, the charging process will have a fast charging time. Slow transient charging can be attributed to the capture of secondary electrons induced from the trapped charges from the fast charging process.

### 5.4 Charge-Trapping Analysis with Constant Voltage Stress Condition

A long-term reliability evaluation was performed under high electric field conditions to verify the interfacial degradation from charge-trapping. Figure 5-4 (a) illustrates the charge-trapping and de-trapping characteristics of two samples during a complete cycle of constant voltage stress at both gate and drain and relaxation cycle. Applied stress conditions were $V_{GS}$ = 2V and $V_{DS}$ = 5V. Threshold voltage shifting ($\Delta V_T$) from trapping in the interface states was evident. Channel carriers are trapped in the defect sites of the $Al_xGa_{1-x}N$ barrier via the interface caused by a high electric field and thin barrier layer[124][130]. The degradation in $V_T$ is consistent with the electron trapping at the $Al_xGa_{1-x}N$ barrier layer defect locations from the GaN channel layer. This trapping phenomenon can be partially recovered by applying recovery voltages of $V_{GS}$ and $V_{DS}$ = 0V. The fast-transient trapping effect, which is active during a short (<1 ms), is accountable for the substantial change of the initial $V_T$ (1s). This effect is caused by the tunneling of channel carriers in the pre-existing defect sites inside the $Al_xGa_{1-x}N$ barrier. The $\Delta V_T$ characteristics at Al = 45% had a higher initial $\Delta V_T$ and more degradation than at Al = 25%.



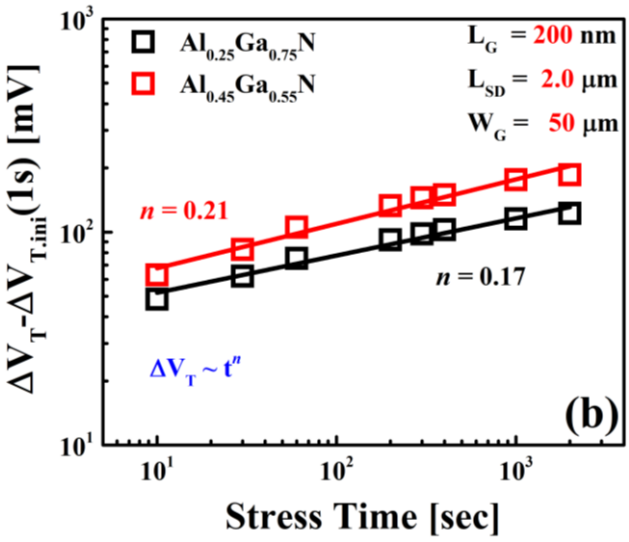



**Figure 5-4 (a)** Threshold voltage shift ($\Delta V_T$) characteristics of AlGaN/GaN HEMTs during constant voltage stress at high drain bias ($V_{DS}$ = 5 V) condition illustrating charge-trapping and de-trapping properties of the channel electrons. **(b)** Power-law time dependency of the observed $\Delta V_T$ excluding the fast-transient charge-trapping components ($\Delta V_T$–$\Delta V_{T.initial\ (1\ s)}$) in two samples.

The time dependence of the $V_T$ was investigated to quantify the charge-trapping phenomenon (figure 5-4 (b)). The fast-transient charge-trapping component, which is supposed to saturate fully after 1 s of stress, may be eliminated, and the power-law equation can be used to describe the time dependence $\Delta V_T \sim t^n$ of the $\Delta V_T$ ($\Delta V_T$ - $\Delta V_{T.initial}$ (1 s))[123][131][125]. Both devices degrade according to the power-law kinetics. Time exponent, *n*, is in the range of 0.17–0.21, a similar but somewhat lower range than for the Al = 25% device, corresponding to a lower interfacial degradation[126]. Regardless of the value of *n*, the $\Delta V_T$ values of Al = 45% devices are much higher than the Al = 25% device associated with higher trap states in the $Al_{0.45}Ga_{0.55}N$ barrier.

### 5.5 Quantitative Analysis of Trap Density

For the quantitative analysis of trap states, we determined the interface ($D_{it}$) and border ($N_{bt}$) trap density for both samples using frequency-dependent C-V characterizations explained in the previous chapter[10]. $D_{it}$ is associated with trap states at the interface of the $Al_xGa_{1-x}N$ barrier and the GaN channel, while $N_{bt}$ is linked to trap states inside the $Al_xGa_{1-x}N$ barrier near the interface[10]. Figure 5-5 (a) illustrates the extracted interface trap density ($D_{it}$) as a function of

the energy level for the samples, which was calculated using the conductance method[87][83]. This method involves utilizing the measured parallel conductance peak $(G_P/\omega)_{max}$ while accounting for the series resistance with a correction[132].

Figure 5-5 demonstrates that a lower Al mole fraction leads to a decrease in the interface trap density due to reduced lattice mismatch with the GaN channel layer. The lowest extracted $D_{it}$ value for the $Al_{0.25}Ga_{0.75}N$/GaN interface was $2.5\times10^{12}$ $cm^{-2}\cdot eV^{-1}$, which is 35% lower than the value of $3.9\times10^{12}$ $cm^{-2}\cdot eV^{-1}$ observed for the $Al_{0.45}Ga_{0.55}N$/GaN interface.

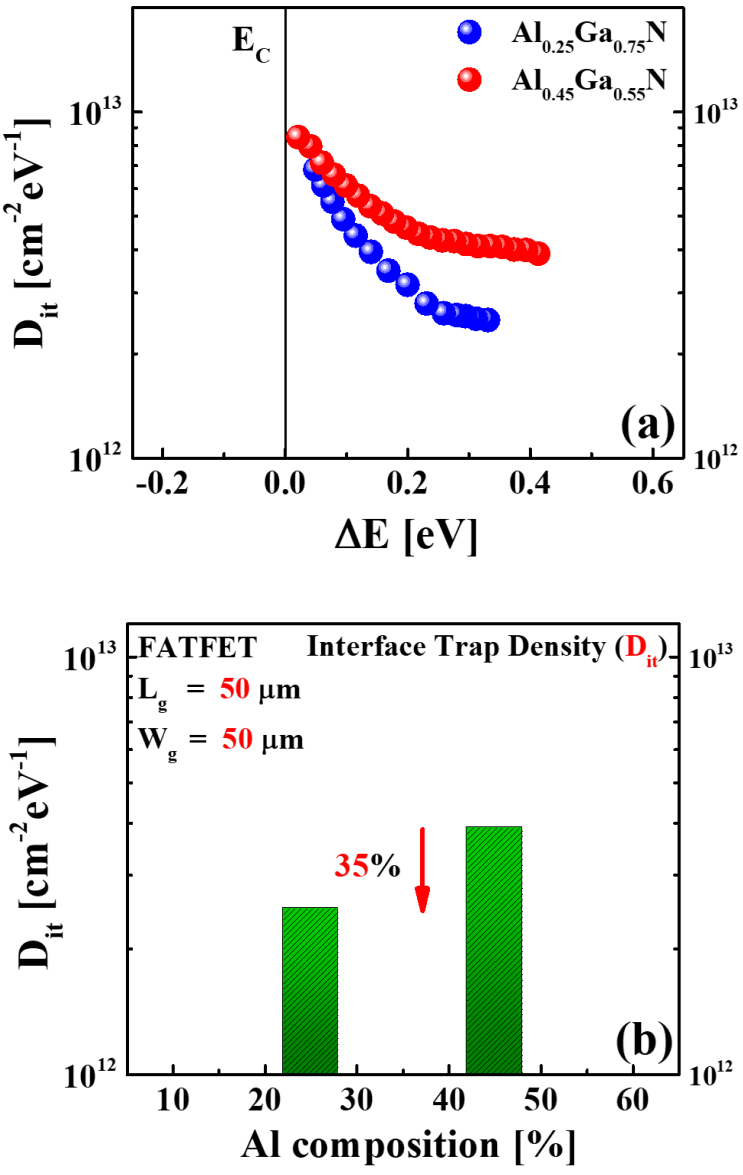
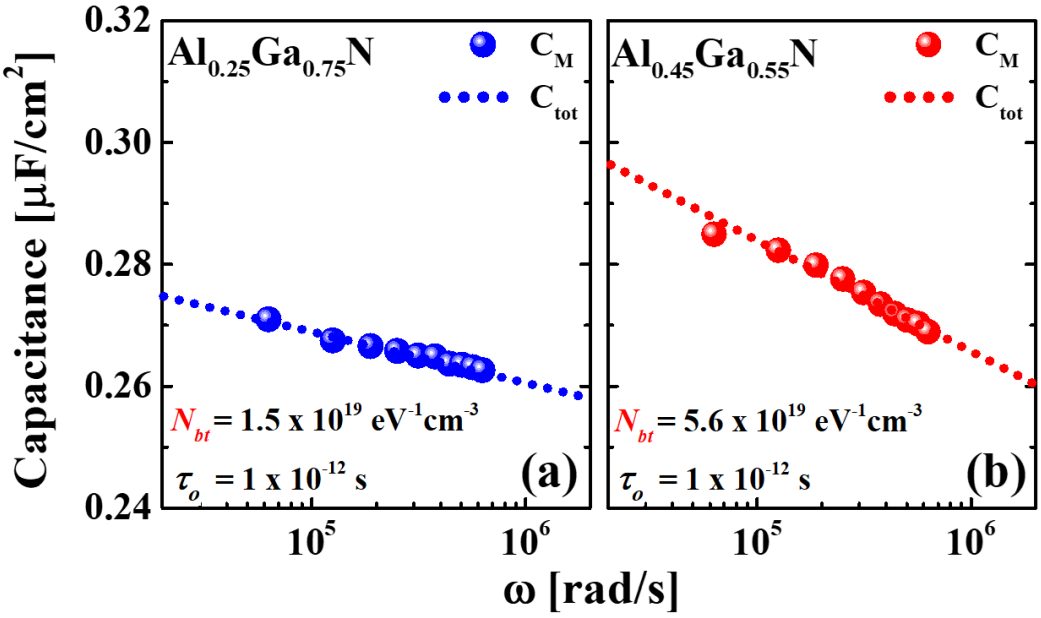



**Figure 5-5 (a)** Interface trap density ($D_{it}$) with respect to band energy with different Al compositions. **(b)** Histogram illustration of interface trap density ($D_{it}$) showing a reduction of 35% with reduced Al composition.

The distributed border trap model, as proposed by Yaun et al., was utilized to determine the border trap density ($N_{bt}$) by identifying the best correspondence between the measured capacitance at a specific voltage in the device accumulation and the capacitance obtained from the model[127][97]. Figure 5-6 (a, b) illustrates the measured ($C_M$) and calculated ($C_{tot}$) capacitances at the accumulation voltage of $V_{GS}$-$V_T$ = 1V and different frequencies while $N_{bt}$ and $\tau_o$ are treated as fitting parameters. By obtaining the best-fitted curves, the values of $N_{bt}$ were extracted. The $Al_{0.25}Ga_{0.75}N$/GaN device exhibited a significantly lower $N_{bt}$ value of 1.5 × $10^{19}$ $cm^{-3}$·$eV^{-1}$, which is 73% lower compared to the $Al_{0.45}Ga_{0.55}N$/GaN device's value of 5.6 × $10^{19}$ $cm^{-3}$·$eV^{-1}$, as shown in figure 5-6 (c). The higher values of $D_{it}$ and $N_{bt}$ for $Al_{0.45}Ga_{0.55}N$/GaN devices align with the pulsed $I_D$-$V_D$ reliability characterization explained earlier.



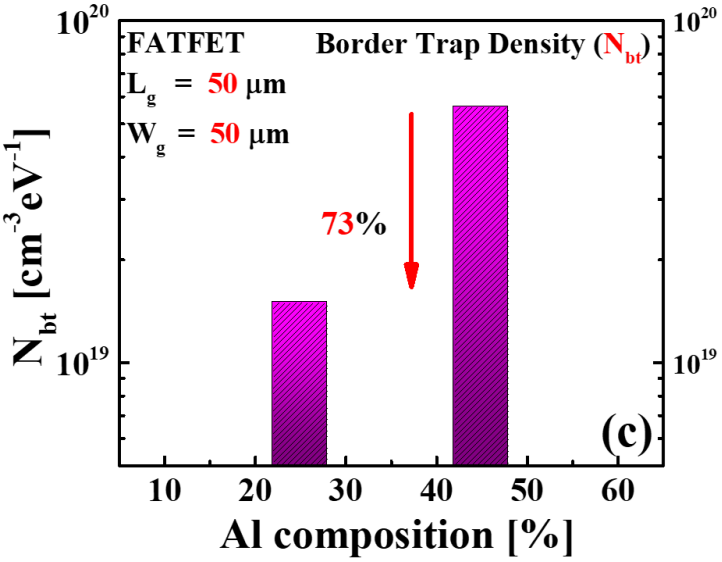



**Figure 5-6 (a)** Fitting curves of measured ($C_M$) and calculated ($C_{tot}$) capacitances at $V_{GS}$-$V_T$ = 1V, generated from the Distributed circuit model. **(b)** Border trap density ($N_{bt}$) with respect to different Al compositions shows a 73% reduction.

We have also analyzed volume trap density ($N_t$) with the 1/*f* low-frequency noise characterizations. We utilized the carrier mobility fluctuation model (CMF) explained in section 3.3.3 for the trap density extraction. The *1/f* noise measurements were performed from 1 Hz to 10 kHz at a fixed drain bias of $V_{DS}$ = 0.5 V from off-state to accumulation, including the linear region. Figure 5-7 (a) illustrates the normalized power spectral density ($S_{ID}/I_D^2$) with respect to the frequency at $V_{GS} = V_T$ condition. The power-law equation ($1/f^{\gamma}$ function) is used to explain the frequency dependency of power spectral density (PSD). $1/f^{\gamma}$ function was fitted with the measured data over the

**Table 5-1** Comparison of Key Reliability Parameters in AlGaN/GaN HEMTs.

| Parameters/Samples | $Al_{0.25}Ga_{0.75}N$/GaN | $Al_{0.45}Ga_{0.55}N$/GaN |
|---|---|---|
| $\Delta I_D$ [mA/mm] | 20 | 67 |
| $n$ | 0.17 | 0.21 |
| $\gamma$ | 1 | 1.3 |
| $D_{it}$ [$cm^{-2}.eV^{-1}$] | $2.5 \times 10^{12}$ | $3.9 \times 10^{12}$ |
| $N_{bt}$ [$cm^{-3}.eV^{-1}$] | $1.5 \times 10^{19}$ | $5.6 \times 10^{19}$ |
| $N_t$ [$cm^{-3}\cdot eV^{-1}$] | $1.8 \times 10^{19}$ | $3 \times 10^{19}$ |

frequency range of 1 Hz to 10 kHz to extract the value of the frequency component (γ)[133]. Based on Table 1, the value of γ is in the range of 1–1.3 (near 1), indicating that the defects/traps had uniform depth and energy[134]. Al = 45% devices had a γ value of 1.3 (Over 1), indicating that the most dominant trap locations are close to the interface of the $Al_{0.45}Ga_{0.55}N$ barrier and GaN channel.

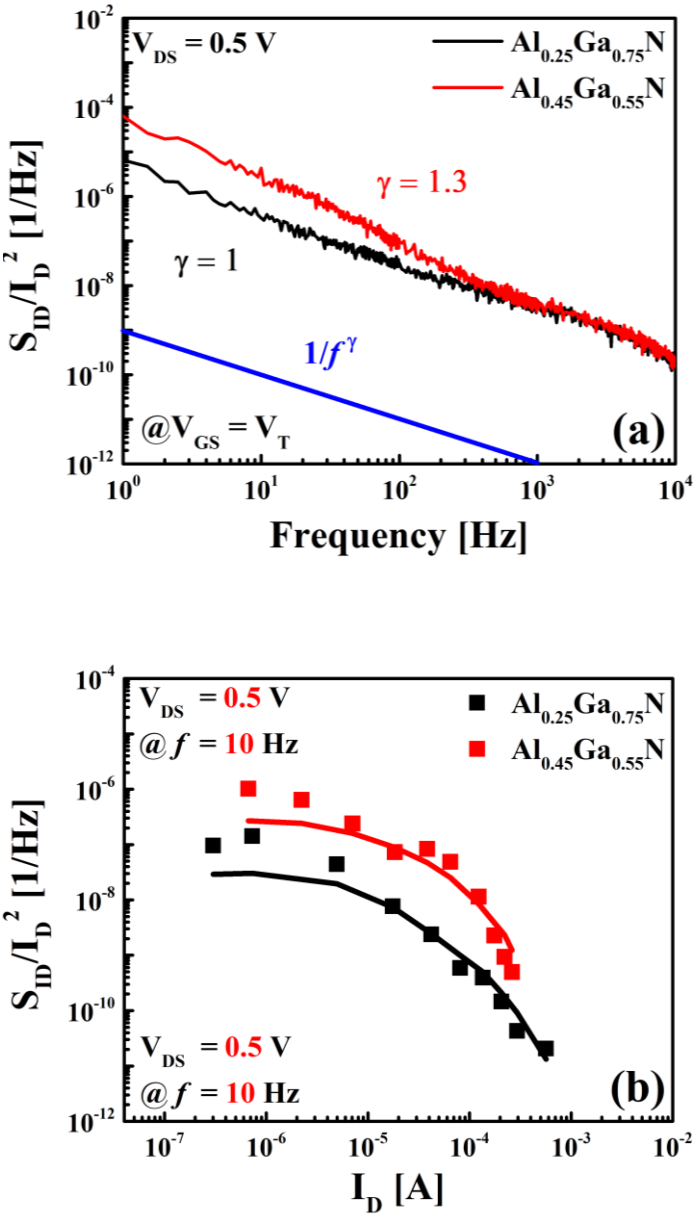
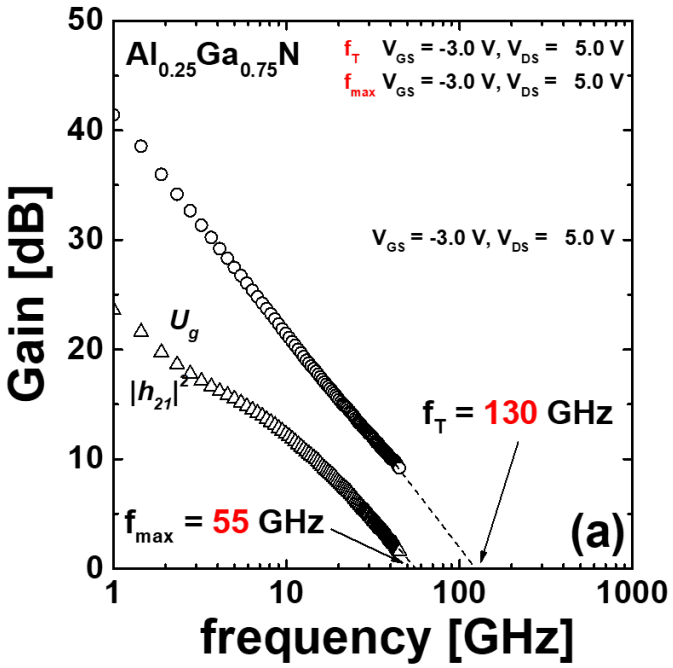



**Figure 5-7 (a)** Comparison of the normalized drain-current power spectral density (PSD) ($S_{ID}/I_D^2$) at $V_{GS} = V_T$ and $V_{DS}$ = 0.5 V. **(b)** Fitting curves of $S_{ID}/I_D^2$ values using the CMF model calculated at a frequency of 10 Hz.

Figure 5-7 (b) illustrates a good fitting between the normalized drain-current power spectral density ($S_{ID}/I_D^2$) and the right side of equation 3.15, which prevails in the CMF model. Using equation 3.16 and the $S_{Vfb}$ extracted from the fitting, $N_t$ for both devices was extracted. Al = 45% devices had a 40% higher $N_t$ value of $3 \times 10^{19}$ $cm^{-3} \cdot eV^{-1}$ compared with $1.8 \times 10^{19}$ $cm^{-3} \cdot eV^{-1}$ for the Al = 25% devices. The reason for these noise characteristics is attributed to the fact that the $Al_{0.45}Ga_{0.55}N$/GaN interface creates higher defect sites near the interface, which increases the probability of the channel electron tunneling into the AlGaN barrier layer.

### 5.6 Microwave properties

To assess the influence of trapping on the microwave properties of the sample, we conducted RF characterizations in the frequency range of 1 to 45 GHz. A Precision Network Analyzer (PNA) system was employed for these measurements, with off-wafer calibration. To account for parasitic pad components, we used on-wafer open and short patterns for data de-embedding[135]. The measured short-circuit gain ($|h_{21}|^2$) and Mason's unilateral gain ($U_g$) for the samples were determined at peak $g_m$ biasing conditions, as depicted in Figure 5-8 (a) & (b). By employing a least-squares fit and



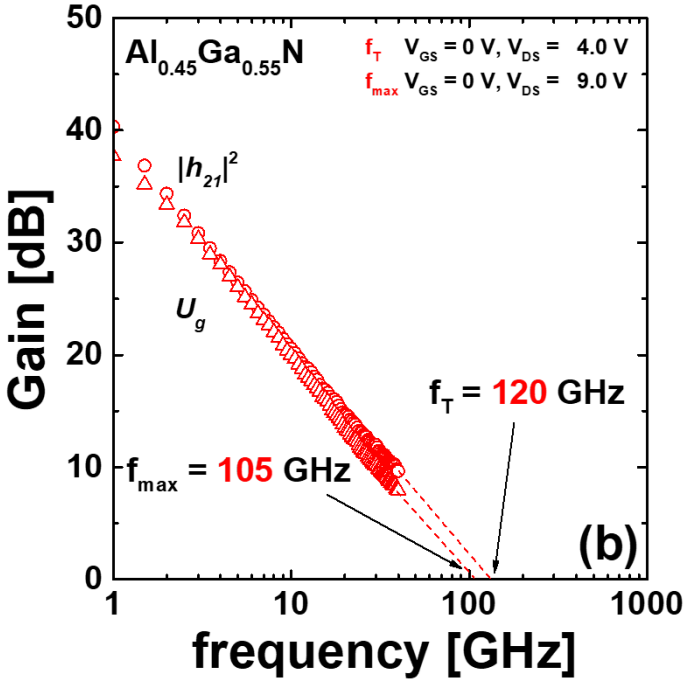



**Figure 5-8** Measured RF Gains ($|h_{21}|^2$, $U_g$) as a function of frequency, at near the peak $g_m$ bias conditions for **(a)** $Al_{0.25}Ga_{0.75}N$ device **(b)** $Al_{0.45}Ga_{0.55}N$ device.

extrapolating the measured data with a slope of -20 dB/dec, we derived the values of $f_T$ and $f_{max}$ for the samples. For Al = 25/45 % devices, the obtained $f_T$ values were 130/120 GHz, while the $f_{max}$ values were 55/105 GHz, respectively. Though Al = 25% shows better reliability in terms of trapping characteristics, but lower lattice mismatch between AlGaN and GaN results in lower 2DEG formation in the channel which can significantly limit microwave properties. Here, both the devices showed similar $f_T$ but Al = 25 % devices exhibited a substantial reduction in $f_{max}$, which can be attributed to the less carrier transport.

### 5.7 Summary

In this chapter, an in-depth trapping characteristic analysis of the $Al_xGa_{1-x}N$/GaN interface of AlGaN/GaN HEMTs based on the variation of Al composition in the $Al_xGa_{1-x}N$ barrier and how it affects device performance were presented. Higher $I_D$ degradation for the $Al_{0.45}Ga_{0.55}N$/GaN devices during the pulsed $I_D$-$V_D$ characterization was attributed to the higher fast-transient trapping in the $Al_{0.45}Ga_{0.55}N$/GaN interface and reliability instability. During constant voltage stress conditions, the $Al_{0.45}Ga_{0.55}N$/GaN device had a higher $V_T$ shift corresponding to higher trapping in the $Al_{0.45}Ga_{0.55}N$ barrier. A larger time exponent $n$ in the

$Al_{0.45}Ga_{0.55}N$/GaN device indicated higher interfacial degradation. During quantitative extraction of $D_{it}$, $N_{bt}$ and $N_t$, the $Al_{0.45}Ga_{0.55}N$/GaN device showed relatively higher trap density, further verifying the higher trapping phenomena in the $Al_{0.45}Ga_{0.55}N$ barrier caused by the rougher $Al_{0.45}Ga_{0.55}N$/GaN interface. These results demonstrate that trapping effects, which impact device performance considerably, are influenced primarily by the quality of the interface between the AlGaN and GaN layers. While it's true that some applications of GaN HEMT devices can potentially benefit from improved device properties achieved by reducing the aluminum (Al) content to reduce lattice mismatches, it's important to note that a substantial reduction in Al content leads to a decrease in the two-dimensional electron gas (2DEG) concentration within the GaN channel layer. This reduction can have a notable impact on carrier transport and, subsequently, on the transconductance ($G_m$). Furthermore, these effects can significantly influence the RF performance of the devices, causing reductions in both the cutoff frequency ($f_T$) and maximum oscillation frequency ($f_{max}$). In the upcoming chapters, we will explore methods to enhance device quality without the need to reduce the Al content, thus ensuring the maintenance of high $f_T$ and $f_{max}$.

# Chapter 6

# Effects of $O_2$ Plasma treatment on Trap states

## 6.1 Introduction

In this chapter, a detailed analysis of the volume/bulk trap, as well as the surface-related trapping phenomena involved in the degradation of RF transconductance ($g_m$) compared to DC transconductance ($G_m$) is presented. To this end, $O_2$ plasma treatment was employed before the deposition of the gate metal on top of an AlGaN layer to improve the bulk, as well as the surface trapping states. The $O_2$ ions not only passivated the AlGaN gate surface area but also penetrated into the bulk and formed Al–O and Ga–O bonds, while treating the volume trap states. In addition, current–collapse effects were improved which ultimately increased the microwave output performances.

## 6.2 $O_2$ Plasma Treatment Technology

Two samples were prepared using the same process flow with a 3–inch wafer. Half of the sample was prepared without any treatment before the gate metal deposition, whereas the other half was subjected to $O_2$ plasma treatment before the gate metal deposition. Epitaxial layers were grown on top of a 4H–SiC substrate using metal–organic chemical vapor deposition in the following sequence: 270 nm of an AlN buffer layer, 400 nm of an $Al_{0.08}Ga_{0.92}N$ back barrier, 40 nm of GaN channel, ~1 nm of an AlN spacer, and 8 nm of an $Al_{0.45}Ga_{0.55}N$ barrier layer. The mesa isolation process was performed using $Cl_2$-based inductively–coupled–plasma (ICP) etching. Subsequently, the substrate was cleaned using an HCl and deionized water (1:5) mixture for 30 s to remove native oxide. To achieve the formation of an ohmic contact, a Ti/Al/Ni/Au (25/160/40/100 nm) alloy was deposited using an electron beam (e–beam) evaporator followed by rapid thermal annealing at 830 °C under ambient $N_2$ flow for 30 s. To achieve a good probe contact, a padding layer of Ti/Au (20/300 nm) was also deposited using an e–beam evaporator.

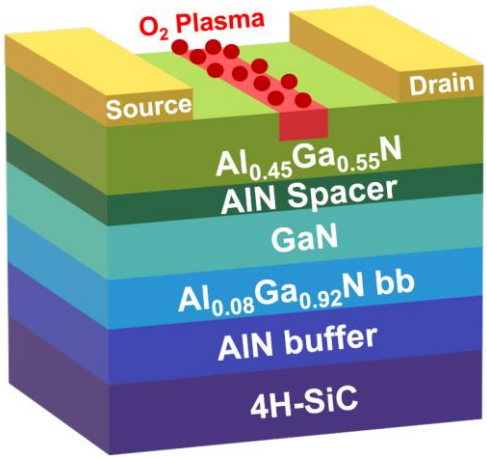



**Figure 6-1** Schematic cross-section showing the effects of the $O_2$ plasma treatment on the bulk of AlGaN barrier layer.

**Table 6-1** Plasma treatment conditions used in this study.

| RIE Power | Pressure | $O_2$/Ar flow | Time | DC bias |
|---|---|---|---|---|
| 33 W | 50 mTorr | 100/5 sccm | 30 s | 126 V |

The contact resistance ($R_c$) from TLM measurements was found to be 0.28 Ω.mm. The gate pattern was defined using electron (e)-beam lithography, and then one of the samples was placed in a reactive ion etching (RIE) chamber for plasma treatment under RIE power of 33 W, chamber pressure of 50 mTorr, and $O_2$/Ar gas flow at a flow rate of 100/5 sccm for 30 s at room temperature which retained a good DC bias of 126 V. Fig. 1a illustrates the schematic of the $O_2$ plasma-treated AlGaN/GaN HEMT. A 'Van Der Pauw" pattern was utilized to conduct hall measurements of the samples. Plasma treatment improved hall mobility ($\mu_{n\_Hall}$), sheet charge density (2DEG), and sheet resistance ($R_{SH}$) from 2100 $cm^2$/V-s, 7.35 × $10^{12}$ $cm^{-2}$, and 400 Ω/□ to 2200 $cm^2$/V-s, 8.58 × $10^{12}$ $cm^{-2}$, and 325 Ω/□ respectively. Lastly, a T-shaped gate of Ni/Au (20/400 nm) was deposited using an e–beam evaporator. Drain–to–source distance was kept fixed at 2µm with gate–to–source and gate–to–drain distances being symmetric. Reduced channel resistance ($R_{CH}$) has an impact on the sample's overall $R_{SH}$. It is possible to define $R_{CH}$ as the sheet resistance beneath the gate in the channel area and can be easily extracted via slope of the linear fit of $R_{ON}$-$L_G$[136]. From our devices, extracted $R_{CH}$ at $V_{GS}$ 1V for as grown sample was 465 Ω/□ and for the $O_2$ plasma treated sample was 375 Ω/□. Around 19.3% reduction was observed in the $R_{CH}$, which is in the similar range as the $R_{SH}$ reduction of 18.75% from hall measurements.

### 6.3 Surface morphology

To further understand the effect of $O_2$ plasma treatment on the AlGaN barrier layer, X-ray photoelectron spectroscopy (XPS) and high-resolution X-ray diffraction (HR–XRD) characterizations were performed. XPS analysis was performed to investigate the variations in the compositions of the barrier layer. The Al 2p and Ga 3d spectra of the barrier layer are shown in Figure 6-2. The intensity of the peaks corresponding to native Ga–O bonds was very low in

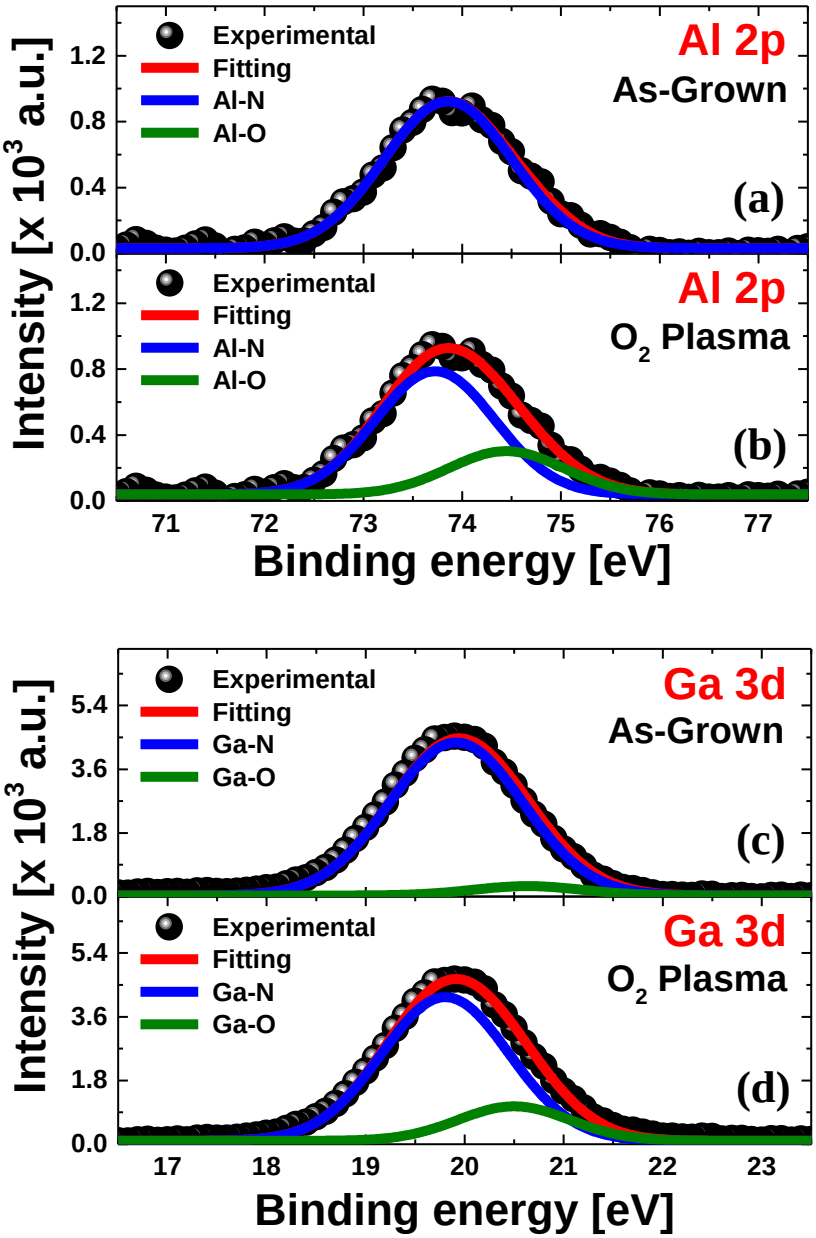



**Figure 6-2 (a,b)** Al 2p and **(c,d)** Ga 3d core-level spectra of the as-grown and $O_2$ plasma-treated samples.

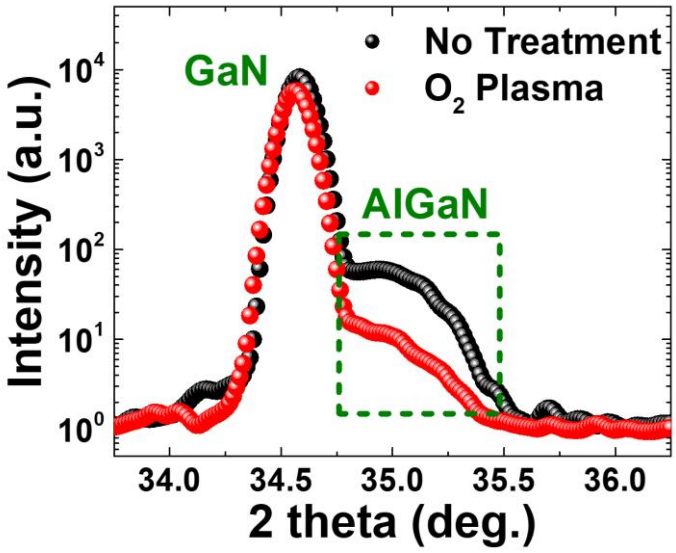



**Figure 6-3** Comparison of the high-resolution X-ray diffraction (HR–XRD) ($\omega$–$2\theta$) profiles of the as-grown and $O_2$-plasma treated samples.

the XPS spectrum of the as-grown sample, whereas no peak corresponding to native Al–O bonds was detected. However, after $O_2$ plasma treatment, the peak of Al–O bonds, as well as an increase in the peak intensity of Ga–O bonds were observed. The higher peak intensity of Al–O, and Ga–O suggests the partial oxidization of the AlGaN layer via the formation of an AlON/GaON compound bond[137][138].

This assumption can be further justified using HR–XRD, and the HR-XRD results are shown in Figure 6-3. A significant reduction in the intensity of the AlGaN peak was observed in the HR-XRD profile of the plasma-treated sample, suggesting a bulk effect of the $O_2$ plasma treatment. It can be assumed that the oxygen ions bond with Al and Ga ions to form Al–O and Ga–O bonds, thus reducing the Al–N and Ga–N bonds[137].

### 6.4 DC characteristics

Table 6-2 summarizes the key device parameters for $L_g$=150nm devices. $O_2$ plasma treatment affected the interface of the gate metal and AlGaN barrier layer. Figure 6-4 (c) shows the leakage current comparison of the samples with both drain and source grounded. It is clearly evident that $O_2$ plasma helped to reduce the gate leakage current. The Schottky barrier height, ideality factor, and leakage current were improved from 0.9 eV, 1.8, and $3\times10^{-7}$ mA/mm to 0.95 eV, 1.6, and $1\times10^{-7}$ mA/mm respectively. Off-state breakdown voltage was also improved from 66 V to 76 V at $V_{GS}$ = -7V, which is demonstrated in Figure 6-4 (d). Figure 6-4 (a) and (b) show the effect of $O_2$ plasma treatment on the drain current–collapse of the samples under different drain–stress biases. The blue, red, and black current data were measured by reverse sweeping drain bias voltages from 10, 15, and 20V to 0V respectively[139]. A drain–current collapse was observed in the as-grown sample with increasing reverse–sweep drain bias (Figure 6-4 (a)). Even though the major cause of the current collapse is the traps between the gate and drain area, there are other possible mechanisms of the current collapse such as the deep levels in the barrier layer (AlGaN) under the gate metal[70]. This method mainly characterizes/gives information on the intrinsic gate region effects for the current collapse. $O_2$ plasma treatment completely reversed this deterioration, and no drain current-collapse was observed during this short period of stress (Figure 6-4 (b)).

**Table 6-2** Comparison of key device parameters for $L_G$ = 150 nm

| Sample | $I_{D\_max}$ @$V_{DS}$=20V [mA/mm] | $I_{Leak}$ @$V_{GS}$=-10V [mA/mm] | $V_T$ [V] | SBH [eV] | IF, n | $V_{BD}$ @$V_{GS}$=-7V [V] |
|---|---|---|---|---|---|---|
| As–grown | 580 | $3\times10^{-7}$ | -2 | 0.9 | 1.8 | 66 |
| $O_2$ plasma | 720 | $1\times10^{-7}$ | -1.92 | 0.95 | 1.6 | 76 |

This suggests that traps in the intrinsic gate region could potentially contribute to the current–collapse. Additionally, electron leakage from the gate into the gate-drain surface area can increase negative potential (in the surface) and create a virtual gate that partially controls current collapse by exchanging charges[64]. $O_2$ plasma treatment passivates the intrinsic gate region and prevents electron leakage, thus mitigating the current collapse.

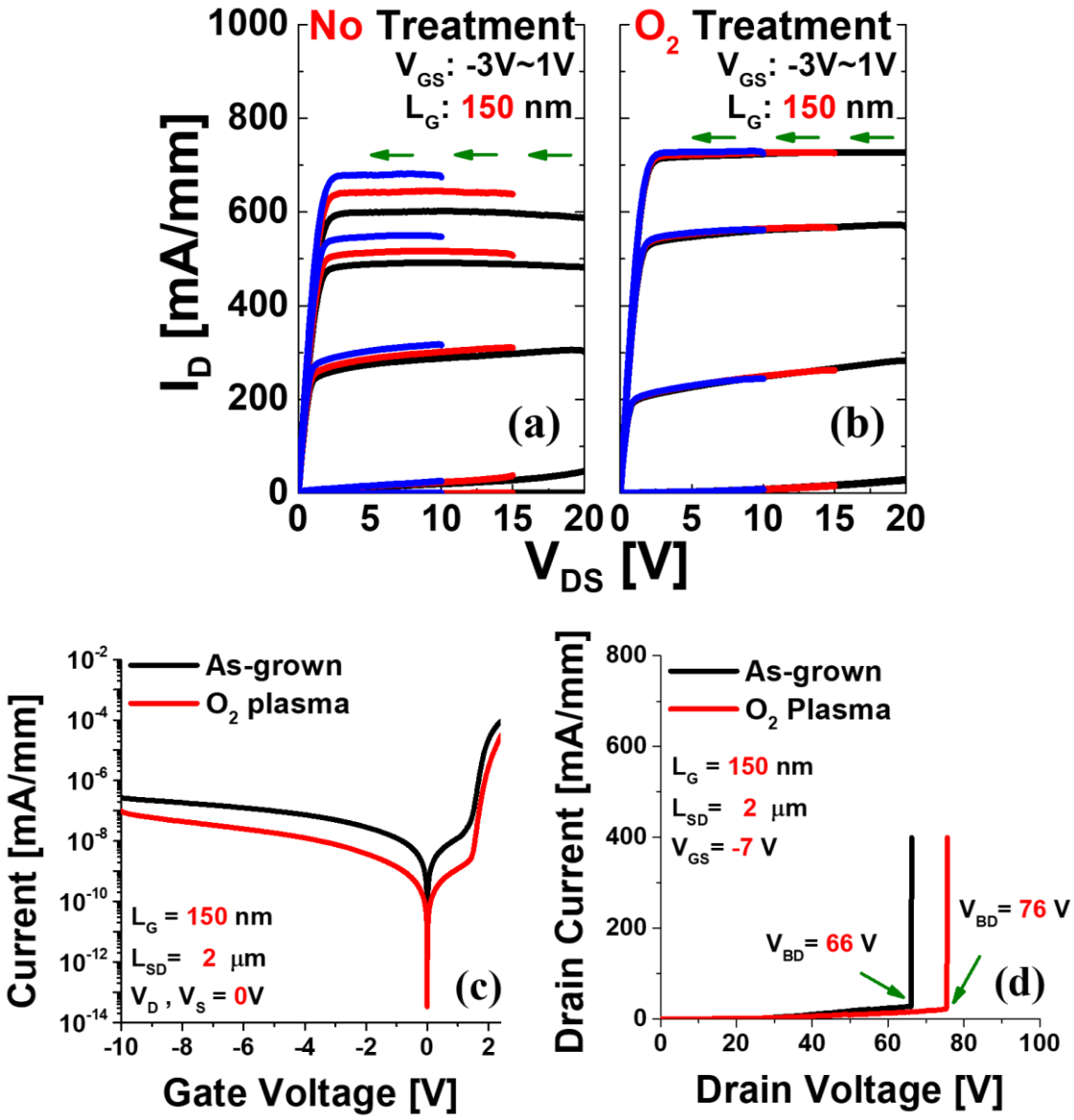



**Figure 6-4** Drain current characteristics under different reverse–sweep drain–stress bias conditions of the **(a)** as–grown and **(b)** plasma–treated samples. **(c)** Leakage Current and **(d)** Off-state break-down voltage comparison between the samples for $L_g$ = 150 nm devices.

### 6.5 Pulsed I-V and Charge Trapping Analysis

Figures 6-5 (a) and (b) show the short single–pulse $I_D$–$V_{GS}$ and $I_D$–time characteristics of the as–grown and $O_2$ plasma-treated samples which were characterized with Keysight B1500A Semiconductor Parameter Analyzer with B1530A waveform generator module. To achieve fast transient trap–free $I_D$–$V_{GS}$ characteristics, the pulse rise time (50 ns) was considered very short[95]. Both the pulse–voltage and the pulse–time domains can be used to depict the change

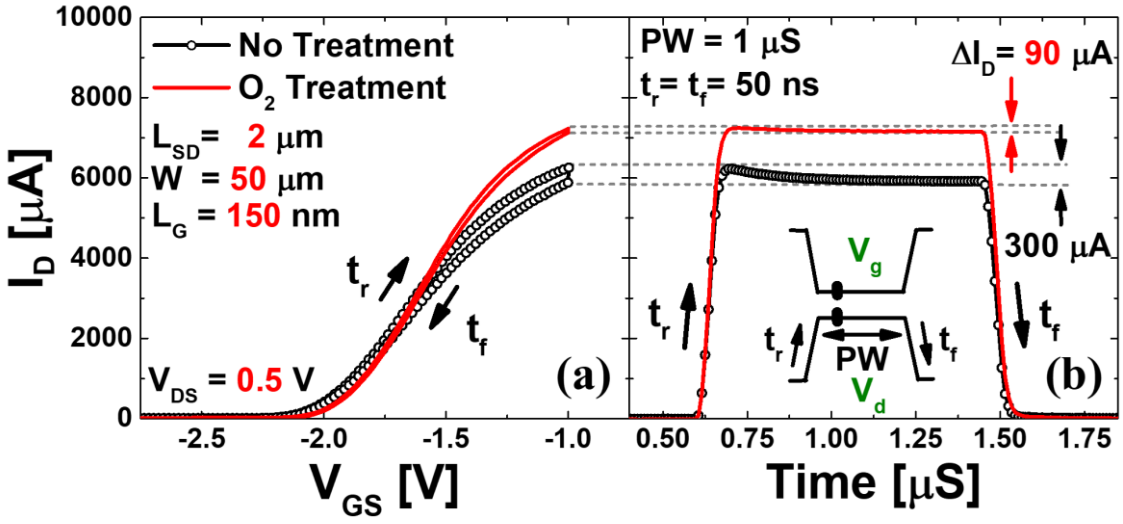



**Figure 6-5 (a)** Single short–pulse $I_D$-$V_{GS}$ measurement data. **(b)** Drain current degradation with respect to time, showing charge trapping.

in $I_D$ during the short single–pulse characterization. In figure 6-5 (b), the inset shows a "single" pulse, in which the $V_G$ pulse and its corresponding $V_D$ responses are recorded and transformed into $I_D$–$V_{GS}$ or $I_D$–time. Hysteresis and drain current degradation over time due to charge trapping were observed in the AlGaN barrier (figure 6-5 (a) and (b)). After $O_2$ treatment, the drain current degradation due to charge trapping reduced significantly (almost 1/3 of that of the as–grown sample). The threshold voltage shift $\Delta V_T$, which is related to the $I_D$ degradation, can also be evaluated using the following expression[95][129][127],

$$\Delta V_T = \frac{\Delta I_D (V_{GS} - V_T)}{I_D} \tag{6.1}$$

Where, $\Delta I_D$ is the total drain current degradation during the short gate pulse, $I_D$ is the trap-less drain current before degradation, $V_{GS}$ is the short gate pulse amplitude, and $V_T$ is the threshold voltage. The $\Delta V_T$ obtained using this expression is identical to the hysteresis value in Figure 6-5 (b). This method provides information on the charge-trapping by obtaining the $\Delta V_T$; however, it cannot provide information on the quantity of the trap density[95].

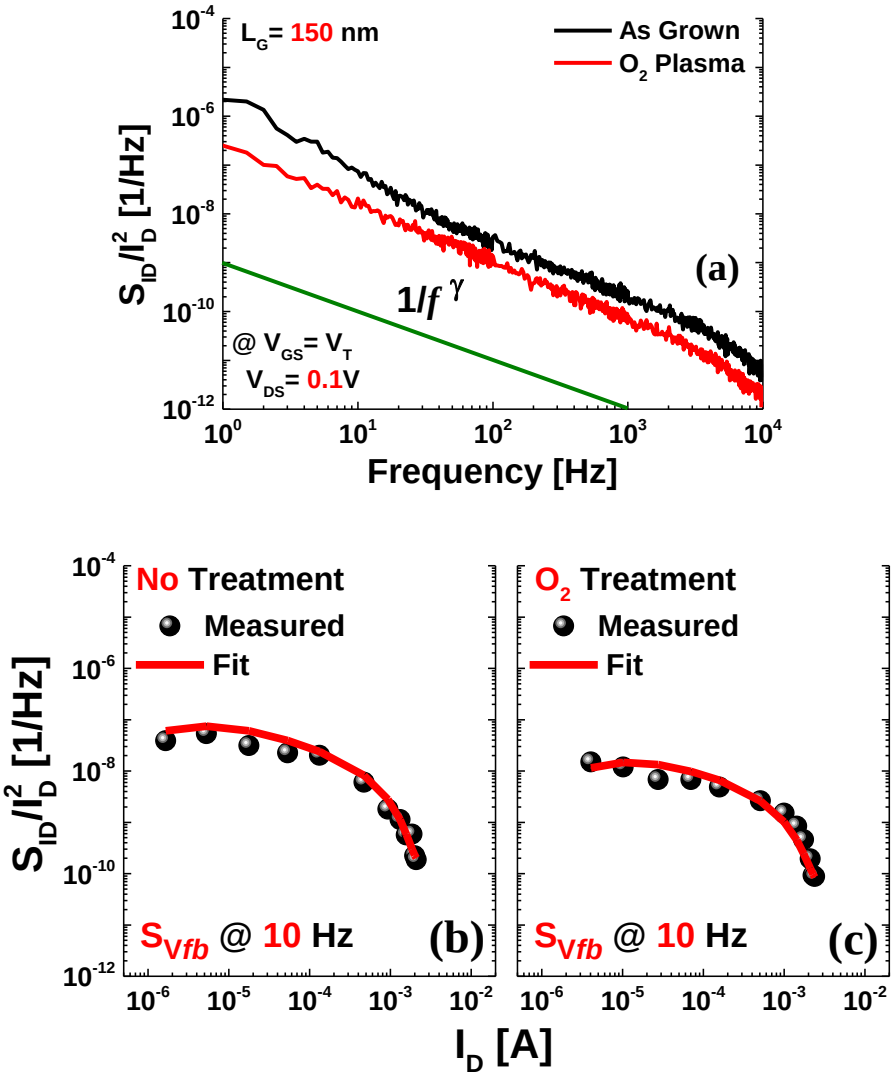



**Figure 6-6 (a)** Normalized power spectral density ($S_{ID}/I_D^2$) vs frequency at $V_{GS} = V_T$ and $V_{DS}$ = 0.1V. Measured and modelled fitting values of noise spectral density ($S_{ID}/I_D^2$) with respect to the drain current ($I_D$) at a frequency of 10 Hz: **(b)** as–grown and **(c)** plasma-treated samples.

To gain further insights into the effect of $O_2$ treatment on the trapping phenomena, 1/*f* low-frequency noise (LFN) characterizations were performed from subthreshold to accumulation at a frequency range of up to $10^4$ Hz and a fixed drain bias ($V_{DS}$ = 0.1 V). Figure 6-6 (a) shows the normalized power spectral density ($S_{ID}/I_D^2$) of the samples with respect to the frequency at $V_{GS} = V_T$. Both samples exhibited $1/f^{\gamma}$ noise characteristics with γ = (1.1–1.2), indicating a constant trap contribution with respect to depth and energy[140][141]. However, compared to the as–grown sample, the $O_2$ plasma-treated samples exhibited lower noise density. With the LNF data, trap characterization was performed using a carrier mobility fluctuation (CMF) model as it provides

accurate and reliable results in all operation regions of a transistor[92][91]. Figure 6-6 (b) & (c) show the normalized power spectrum density at different drain current points for as–grown and plasma-treated samples respectively. Black spheres represent the measured values, while the red line represents the results of the model fitting using the CMF model. A good fitting between the normalized power spectral density $S_{ID}/I_D^2$ and corresponding $(G_m/I_D)^2$ over a wide range of drain current ensures the attribution of LFN to the CMF model. The $S_{Vfb}$ values of the as–grown and $O_2$-treated samples obtained using the model at f =10Hz were $7.32 \times 10^{-11}$ and $2.4 \times 10^{-11}$ $V^2 \cdot Hz^{-1}$, respectively. Using equation 3.16, the $N_t$ values of the as–grown and $O_2$-treated samples were extracted to be $5.3 \times 10^{18}$ and $1.7 \times 10^{18}$ $cm^{-3} \cdot eV^{-1}$, respectively. These results indicate that the $O_2$ plasma treatment resulted in approximately a 67% reduction in the volume trap density of the sample.

### 6.6 RF Characteristics Analysis

The RF characterizations of these samples were performed from 1 to 45 GHz using an HP 8510C Network Analyzer with off–wafer calibration. The de–embedding of the parasitic pad components from the measured S-parameter data was performed using on–wafer open and short patterns. The as–grown sample exhibited significant RF $g_m$ collapse (Figure 6-7 (a) & (b)), whereas the RF $g_m$ value of the $O_2$ plasma–treated sample was almost restored to the expected value, which could be attributed to the significant reduction in the volume trap states. Figure 6-8 (a) and (b) show the measured RF gains [$|h_{21}|^2$, $U_g$ and maximum available gain (MAG)] of both devices with respect to the frequency at $L_g$ = 150 nm and near peak $g_m$ bias at $V_{DS}$ = 10V. The $f_T$ and $f_{max}$ were obtained by extrapolating the short–circuit gain $|h_{21}|^2$ and Mason's unilateral gain, $U_g$, respectively. A complete form of $f_T$ & $f_{max}$ can be given by[142][143]:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})(1+(R_s+R_d)g_d)+g_m C_{gd}(R_s+R_d)} \tag{6.2}$$

$$f_{\max} = \frac{f_T}{2\sqrt{(R_i+R_s+R_g)g_d+(2\pi f_T)R_g C_{gd}}} \tag{6.3}$$

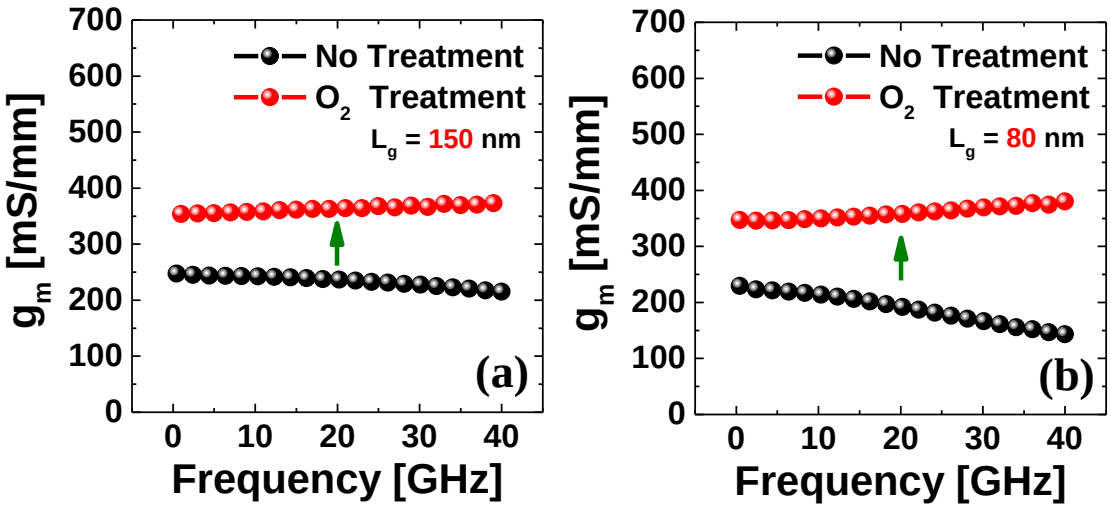
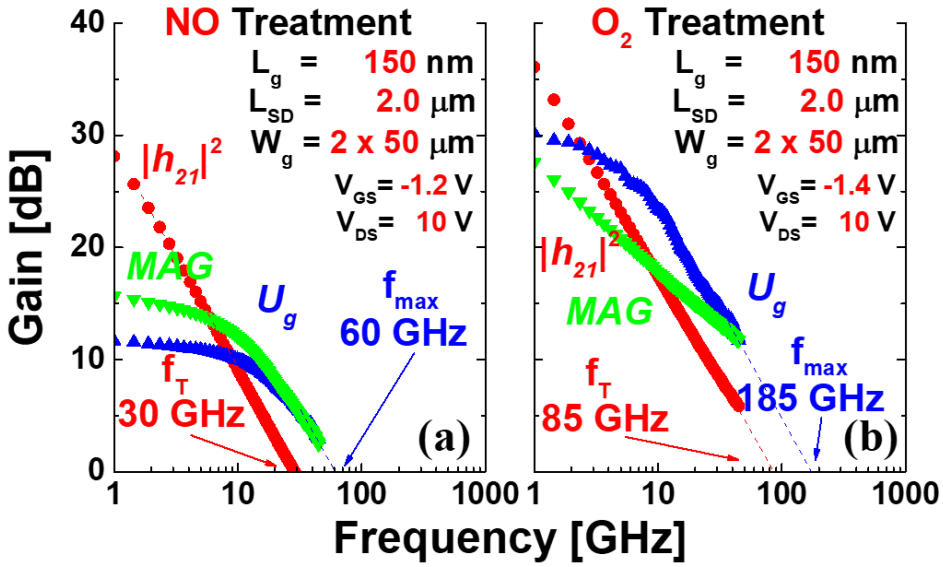



**Figure 6-7** RF $g_m$ of the samples as a function of the frequency **(a)** $L_g$ = 150 nm **(b)** $L_g$ = 80 nm.

The $f_T$ and $f_{max}$ of the plasma-treated sample were 85 and 185 GHz, respectively, which were significantly higher than those of the as-grown sample ($f_T$ and $f_{max}$ of 30 and 60 GHz, respectively), which could be attributed to the reduction in the RF $g_m$ collapse. Reducing $L_g$ to 80 nm significantly increased the $f_T$ and $f_{max}$ even further to 85 and 185 GHz from 65 and 70 GHz respectively, which is shown in Figure 6-8 (c) & (d).



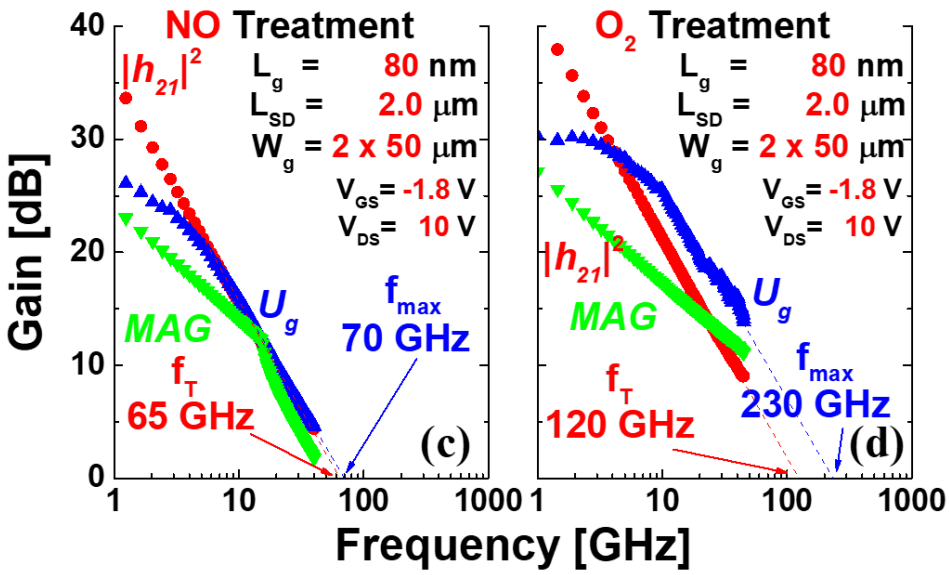
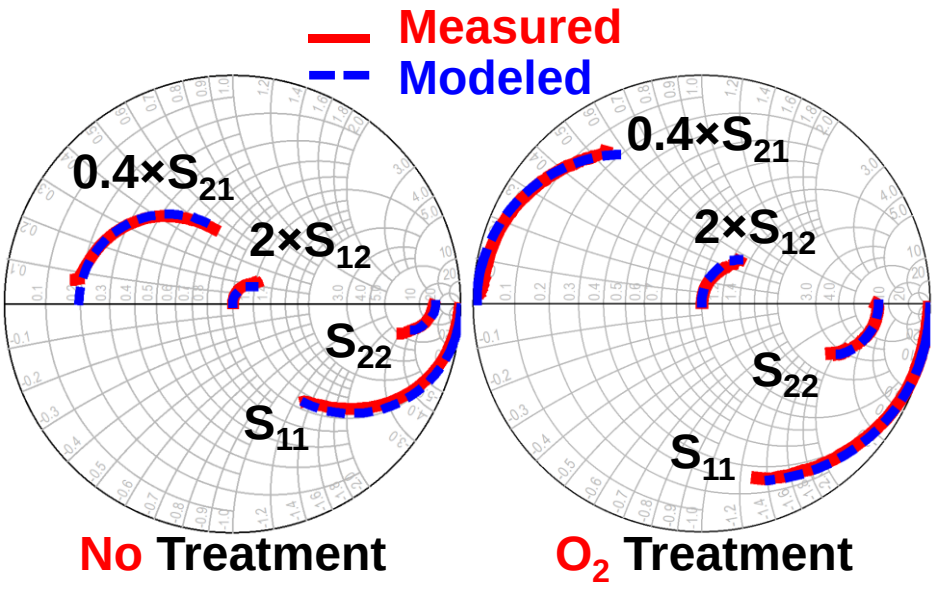



**Figure 6-8** RF Gains as a function of the frequency at $V_{DS}$ = 10V, near the peak $g_m$ gate voltage: **(a)** as–grown $L_g$ = 150 nm **(b)** $O_2$ plasma $L_g$ = 150 nm **(c)** as–grown $L_g$ = 80 nm **(d)** $O_2$ plasma $L_g$ = 80 nm.

Small–signal modeling (SSM) can further explain the physical origins of these excellent improvements in high-frequency characteristics. An SSM analysis of $L_g$ = 80 nm devices has been displayed in Figure 6-9. The parameters table in Figure 6-9 show a significant increase in voltage gain $g_m/g_d$ and a reduction of gate–drain capacitance $C_{gd}$ and gate resistance $R_g$ after plasma treatment. Mostly these parameters depend on the surface and material quality under the gate foot region and act as limiting factors for $f_T$ & $f_{max}$. The significant increase in the $f_T$ & $f_{max}$ could be attributed to the reduction in the $C_{gd}$, and $R_g$, which was caused by a very thin oxide (Ga–O) layer under the gate contact region, produced via oxide dissemination through $O_2$ plasma treatment and ultimately restoring the $g_m$ to the expected level.




| Parameter | No | $O_2$ |
|---|---|---|
| $g_m$ [mS/mm] | 250 | 360 |
| $g_d$ [mS/mm] | 60 | 39 |
| $C_{gs}$ [fF/mm] | 380 | 390 |
| $C_{gd}$ [fF/mm] | 172 | 104 |
| $C_{ds}$ [fF/mm] | 50 | 25 |
| $R_i$ [Ω.mm] | 0.033 | 0.009 |
| $R_g$ [Ω.mm] | 4.3 | 0.5 |
| $R_s$ [Ω.mm] | 0.4 | 0.4 |
| $R_d$ [Ω.mm] | 1.4 | 1 |
| $f_T$ [GHz] | 65 | 120 |
| $f_{max}$ [GHz] | 70 | 230 |

**Figure 6-9** Small-signal modelling analysis for $L_g$ = 80 nm devices at $V_{GS}$ = -1.8V; $V_{DS}$ =10V with measured and modelled data.

A load–pull measurement was conducted on both samples to analyze the RF output characteristics. Fig. 7 shows the results of $L_g$ = 150 nm devices measured at 8 GHz with a drain supply voltage of 25V for both cases. Extracted $P_{out\_max}$ after tuning the input and output impedance for maximum output power for the as-grown sample is around 1.25 W/mm whereas

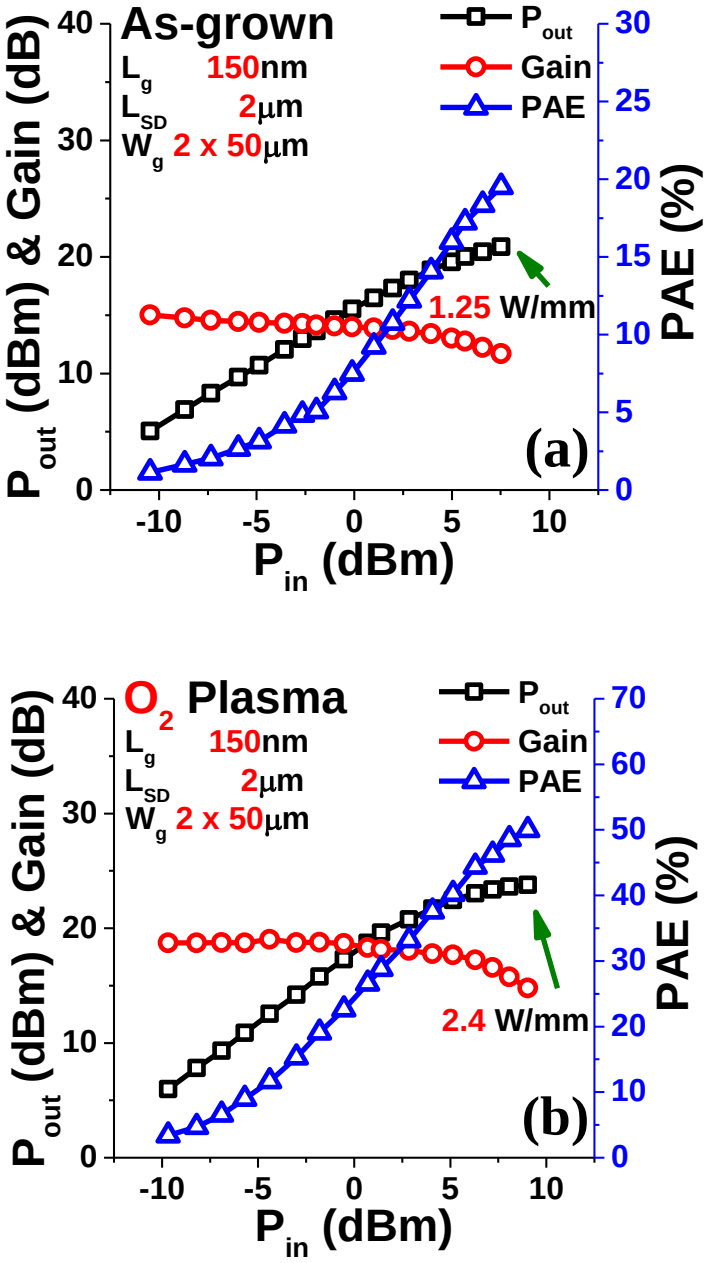



**Figure 6-10** Output power characteristics for $L_g$ = 150 nm devices measured at 8GHz, with a drain bias of $V_{DS}$ = 25V **(a)** As-grown **(b)** $O_2$ Plasma.

for plasma treated sample it is 2.4 W/mm. Power-added efficiency (PAE) and linear gain have also been improved significantly to 50% (from 20%) and 19 dB (from 15 dB) after plasma treatment. Adding a surface passivation layer in the gate–to–drain and gate–to–source region will further improve these performances[144][145]. These results clearly exhibit the impact of plasma treatment on the RF output characteristics.

## 6.7 Summary

In this chapter, we illustrate the impact of $O_2$ plasma treatment before gate metal deposition on the volume trap states in the AlGaN barrier layer of an AlGaN/GaN HEMT and its significant enhancement of device performance. We employed X-ray Photoelectron Spectroscopy (XPS) and High-Resolution X-ray Diffraction (HR-XRD) to probe the bulk effects of the $O_2$ plasma treatment. Our results demonstrate that the $O_2$ plasma-treated sample exhibits superior Schottky characteristics compared to the as-grown sample. While the as-grown sample experienced drain current collapse, the $O_2$ plasma-treated sample maintained a stable $I_D$ under reverse-sweep drain-stress bias conditions. Moreover, short single-pulse and 1/$f$ noise characterizations validate a remarkable 67% reduction in volume trap states due to the plasma treatment, resulting in substantially improved values for $f_T$ and $f_{max}$. Lastly, load-pull analysis underscores the remarkable enhancements in $P_{out\_max}$, Power Added Efficiency (PAE), and linear gain, increasing from 1.25 W/mm, 20%, and 15 dB to 2.4 W/mm, 50%, and 19 dB, respectively, for the $O_2$ plasma-treated sample. In the following chapter, we will delve into the intricacies of Hot Electron Degradation and the measures taken to address and improve this issue.

# Chapter 7

# Trapping effects due to Hot electrons

## 7.1 Introduction

In this chapter, we conducted a comprehensive investigation into the Positive-Bias-Temperature Instability (PBTI) and hot electron trapping behaviors in AlGaN/GaN HEMTs, particularly as we aggressively scaled down the channel thickness. Our study utilized AlGaN/GaN HEMTs, which were nearly identical in design, differing mainly in terms of the channel thickness and the inclusion of an $Al_{0.08}Ga_{0.92}N$ channel back barrier. To analyze trapping phenomena, we subjected the devices to long-term reliability testing, subjecting them to high drain bias and elevated ambient temperatures. In addition, we performed pulsed *I-V* and low-frequency 1/*f* noise characterizations, allowing us to quantitatively estimate trap densities. Finally, we conducted Scattering parameter (S-parameter) measurements to assess how these trapping phenomena influenced the microwave characteristics of the devices. This chapter comprises two main sections: First, we look into the impact of introducing an $Al_{0.08}Ga_{0.92}N$ channel back barrier on mitigating "Hot electron effects". Subsequently, we examine how scaling the channel thickness influences these hot electron effects.

## 7.2 Channel Back Barrier Technology

For this analysis, we prepared 3 samples using similar process conditions explained in the previous chapters. All the samples were grown on a 3–inch semi-insulating SiC wafer. The device schematics are shown in Figure 7-1. One of these devices features a thick channel ($t_{ch}$ = 420nm) without any channel back barrier, while the other two devices possess thin channels ($t_{ch}$ = 40nm & 20nm) and incorporate a channel back-barrier. The epitaxial layers were deposited onto a 4H–SiC substrate using metal-organic chemical vapor deposition. The layer sequence included 270 nm of an AlN buffer layer, 400 nm of an $Al_{0.08}Ga_{0.92}N$ back barrier ($t_{ch}$ = 40nm & 20nm),

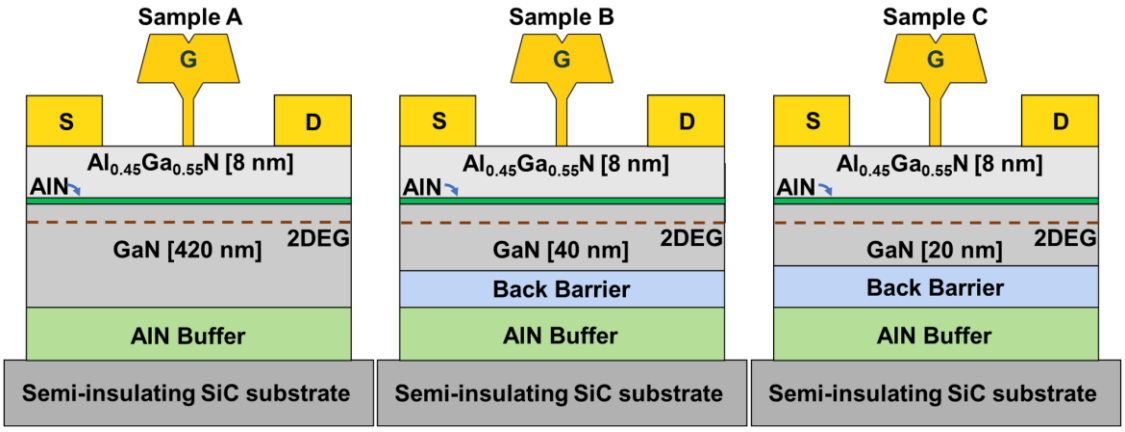



**Figure 7-1** Cross-section schematics of the samples used in this study.

420/40/20 nm of GaN channel, approximately 1 nm of an AlN spacer, and 8 nm of an $Al_{0.45}Ga_{0.55}N$ barrier layer. The processes of mesa isolation, ohmic contact formation, gate deposition, and pad metal formation closely resemble those described in previous sections for similar devices. Additionally, all three devices underwent $O_2$ plasma treatment before the gate deposition.

### 7.2.1 "Hot Electron trapping" mechanism

The trapping mechanism in a fresh device is the primary focus of our examination. By biasing the device in the ON-state, we can observe a trapping transient. The effects of electron trapping in AlGaN/GaN HEMTs are visually depicted in the cross-section and band diagram in Figure 7-2. The generation of "hot electrons" during the on-state is the primary cause of these trapping effects. "Hot electrons" refer to nonequilibrium channel electrons that break atomic bonds, create interface states, or activate traps after gaining sufficient kinetic energy to overcome potential energy barriers. They subsequently inject themselves into the buffer, barrier, or insulating layers, where they become trapped[59]. In addition to hot electrons, there is a built-in lattice mismatch between the GaN channel and the AlGaN barrier/AlN buffer, resulting in significant in-plane tensile stress and stored elastic energy. This stress intensifies when a strong vertical electric field is applied, as GaN and AlN possess strong piezoelectric properties that create defect sites in both the barrier and buffer[146]. These defect sites can function as electrical traps and degrade drain current ($I_D$) and transconductance ($G_m$), thereby significantly impacting device performance.

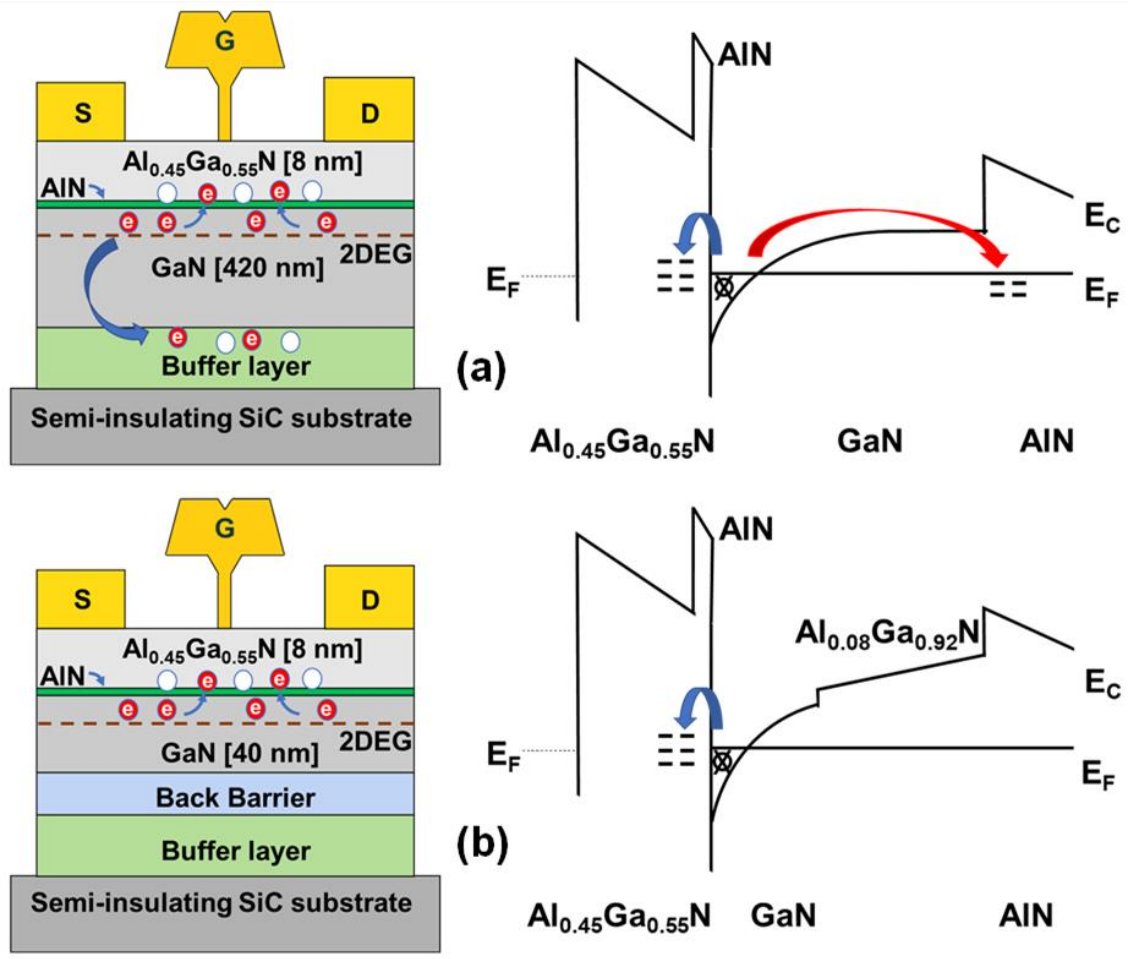



**Figure 7-2** Schematic cross-section and band diagram showing the effects of "Hot electron" trapping in AlGaN/GaN hemts **(a)** $t_{ch}$ = 420 nm without back–barrier **(b)** $t_{ch}$ = 40 nm with back–barrier

In Figure 7-2 (a), a schematic of the thick channel device without a back barrier is shown, where hot electrons can readily tunnel into the AlGaN barrier and buffer, leading to severe degradation of device performance. Conversely, the inclusion of an almost lattice-matched thick $Al_{0.08}Ga_{0.92}N$ channel back barrier (Figure 7-2 (b)) can noticeably reduce hot electron trapping in the buffer and improve electron confinement in the channel, resulting in enhanced device performance.

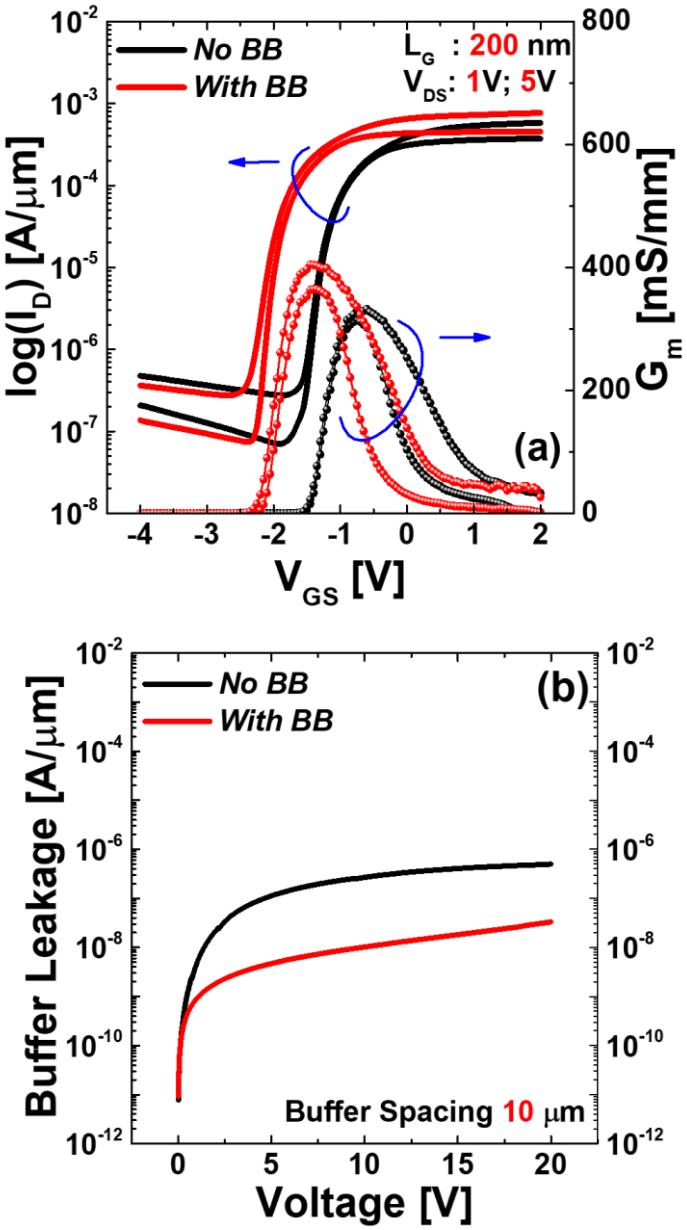



**Figure 7-3 (a)** DC Transfer characteristics ($I_D$ vs $V_{GS}$, $G_m$ vs $V_{GS}$) comparison of the samples. **(b)** Buffer leakage current comparison showing the effect of including back–barrier.

Figure 7-3 (a) displays the DC *I-V* characteristics of the devices, and it's evident that the $t_{ch}$ = 40nm device with the back barrier exhibits a noticeable improvement in drain current ($I_D$) and transconductance ($G_m$). We also examined the buffer leakage current of the devices with a mesa spacing of 10 µm, as demonstrated in Figure 7-3 (b). The inclusion of a back-barrier resulted in a reduction of over one order of magnitude in buffer leakage current, corresponding to a lower degree of trapping in the buffer.

### 7.2.2 PBTI Degradation and $V_T$ Shift Kinetics

To gain deeper insights into trapping effects, we conducted Positive Bias Temperature Instability (PBTI) characterizations. These tests allowed us to assess the long-term reliability under high drain bias conditions. Figure 7-4 (a) showcases the carrier trapping and de-trapping behaviors of the devices during various PBT stress and relaxation cycles. We subjected the devices to three different gate electric field stresses ($V_{GS}$ = 1, 2, 3V) under high drain bias conditions ($V_{DS}$ = 5V) to simulate hot electron trapping at 125°C. The observed deterioration in threshold voltage ($\Delta V_T$) is associated with the electron trapping process occurring at the defect

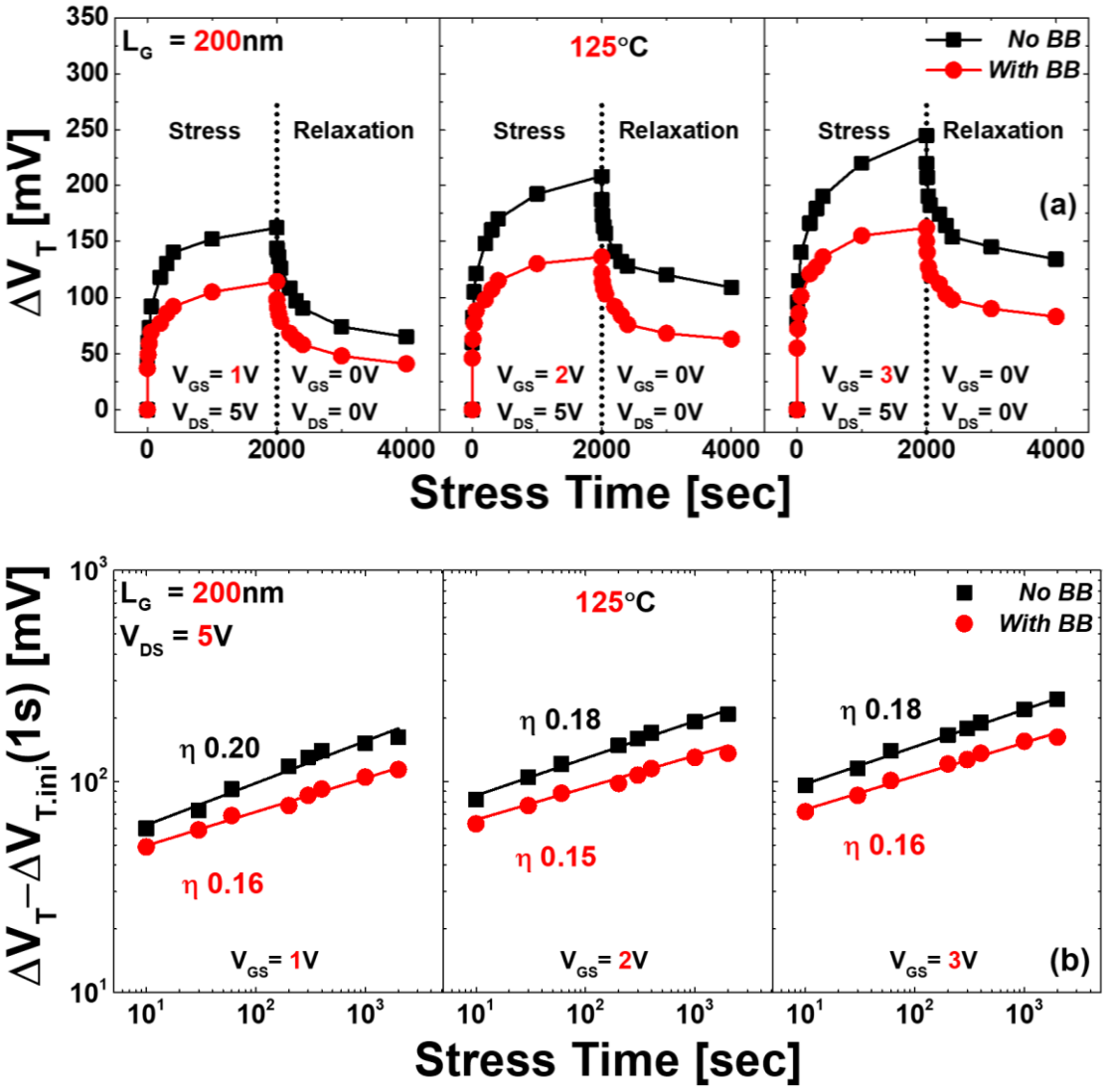



**Figure 7-4 (a)** Threshold voltage shift ($\Delta V_T$) corresponding to stress time showing charge trapping and detrapping phenomena. **(b)** Power-law time dependency of the samples after removing fast transient charging components ($V_T$ - $V_{T.initial}$ (1 s)).

locations [13]. By applying relaxation voltages of $V_{GS}$ and $V_{DS}$ = 0V, we were able to partially recover trapped electrons. The initial high $\Delta V_T$ degradation of the devices, occurring within the first second of stress, is linked to fast-transient charge trapping, which dominates over a short duration (<1 msec) [14]. Notably, the $t_{ch}$ = 40nm device exhibited relatively less fast transient trapping compared to the $t_{ch}$ = 420nm device. This discrepancy is primarily caused by electron tunneling from the GaN channel directly into pre-existing shallow traps within the $Al_{0.45}Ga_{0.55}N$ layer. For a more accurate assessment, it's important to subtract the impact of fast-transient charge trapping from the initial 1-sec stress [14][15].

To quantify the charge-trapping phenomenon, we delved into the time-dependent $V_T$ deterioration. The time evolution of the $V_T$ shift ($V_T$ - $V_{T.initial}$ (1 s)) can be accurately described by a power-law expression, $\Delta V_T \sim t^n$, once we eliminate the fast-transient charge trapping component, which is expected to saturate within 1 s of stress[16]. In Figure 7-4, it's evident that the total threshold voltage deterioration is notably higher for the $t_{ch}$ = 420nm device under different stress conditions. This difference is undoubtedly linked to the hot electron trapping in the buffer layer. Both devices displayed degradation

following power-law kinetics. However, the average time exponent ($n$) for the $t_{ch}$ = 40 nm device ($n$ = 0.15~0.16) is slightly lower than that for the $t_{ch}$ = 420 nm device ($n$ = 0.18~0.20), as shown in Figure 7-4 (b). Although the values of n fall within a similar range, the slightly lower value for the $t_{ch}$ = 40 nm device indicates a lower degree of interfacial degradation[126].

In Figure 7-5, we observe the effective trap density ($\Delta N_{eff}$) for the samples concerning applied stress electric fields at three distinct ambient temperatures. We calculate $\Delta N_{eff}$ using the following equation[147]:

$$\Delta N_{eff} = \frac{\Delta V_T \times C_b}{q} \tag{7.1}$$

It's evident that the total $\Delta N_{eff}$ for the $t_{ch}$ = 420 nm device is relatively higher. The voltage dependency ($y$) of $\Delta N_{eff}$ is a critical attribute impacting the samples' reliability. A weak voltage dependency indicates higher defect levels near the channel Fermi level, leading to channel carrier trapping at low voltages[148]. Although the values of $y$ are quite similar, the $t_{ch}$ = 40 nm device exhibits a better voltage dependency compared to the $t_{ch}$ = 420 nm device. As the ambient

temperature increases, the voltage dependency worsens for both devices, indicating a notable temperature effect on the defect sites.

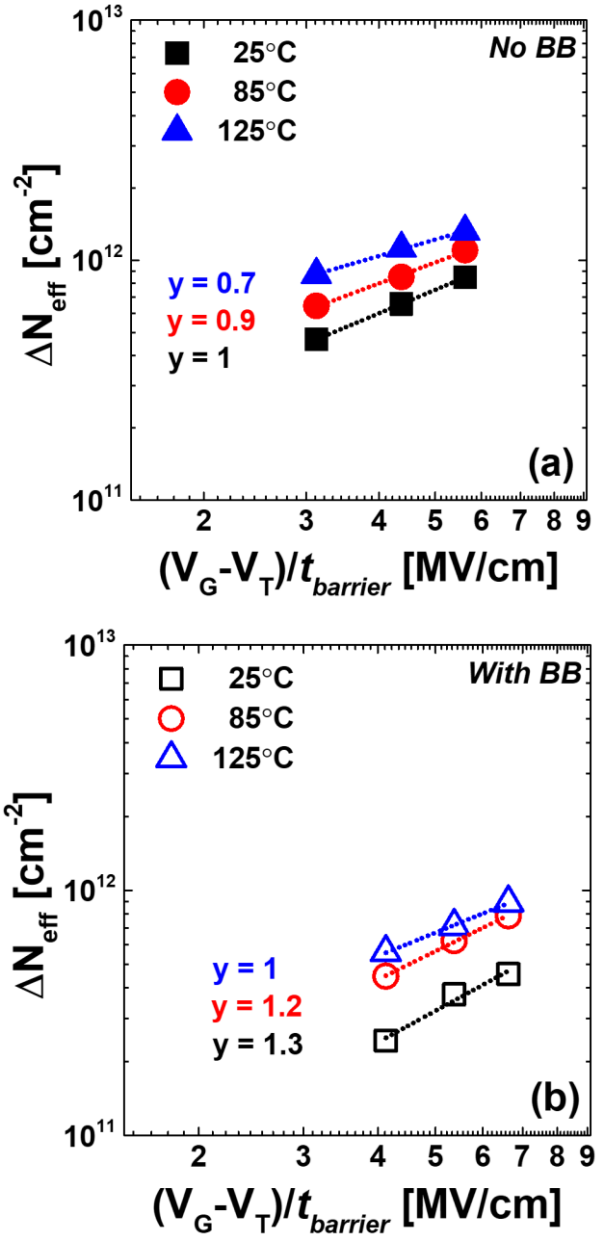



**Figure 7-5** Effective trap density ($\Delta N_{eff}$) with respect to applied stress electric field showing voltage dependency ($y$) of **(a)** $t_{ch}$ = 420 nm without back–barrier **(b)** $t_{ch}$ = 40 nm with back–barrier.

Figure 7-6 displays an Arrhenius plot illustrating the activation energy ($E_a$) for the samples. We measured $\Delta V_T$ after 2000 seconds at three different temperatures (25°C, 85°C, and 125°C) for this analysis. Comparatively, thin channel devices exhibit a more pronounced temperature dependency on the PBTI $V_T$ shift than their thick channel counterparts. Assuming the defect reaction rate is linear with respect to time, and considering time exponents $n$ = 0.15~0.16/0.18~0.20, we extracted the activation energy for $t_{ch}$ = 40/420 nm devices in the range of 0.19~0.23/0.12~0.15, respectively. The improved temperature dependency of $t_{ch}$ = 40 nm devices can be attributed to fewer channel electrons tunneling into the defect sites[149].

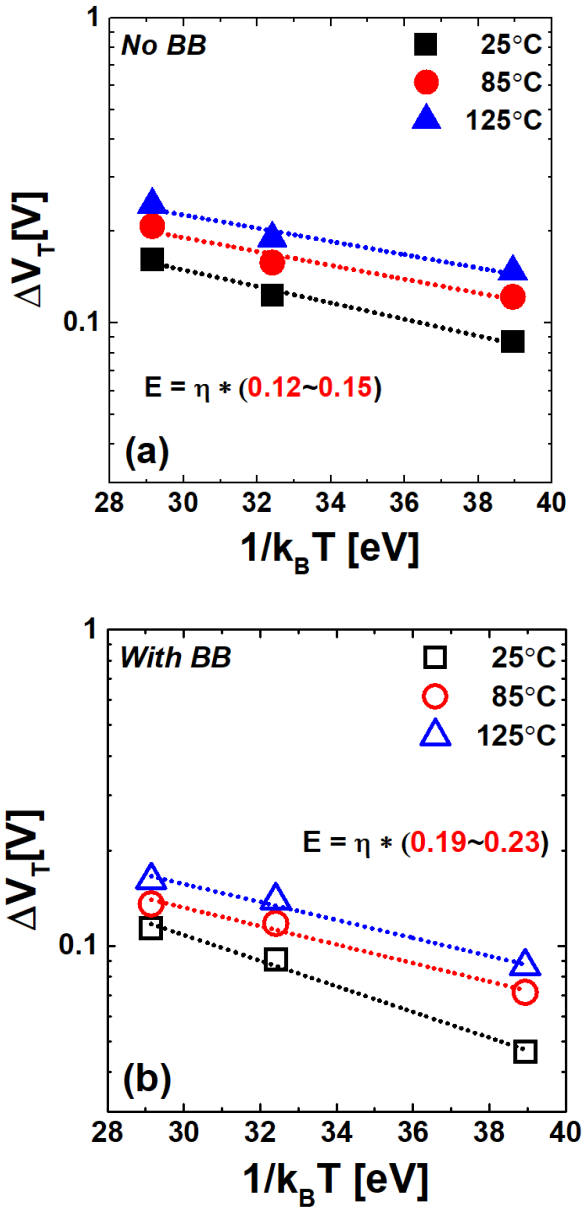
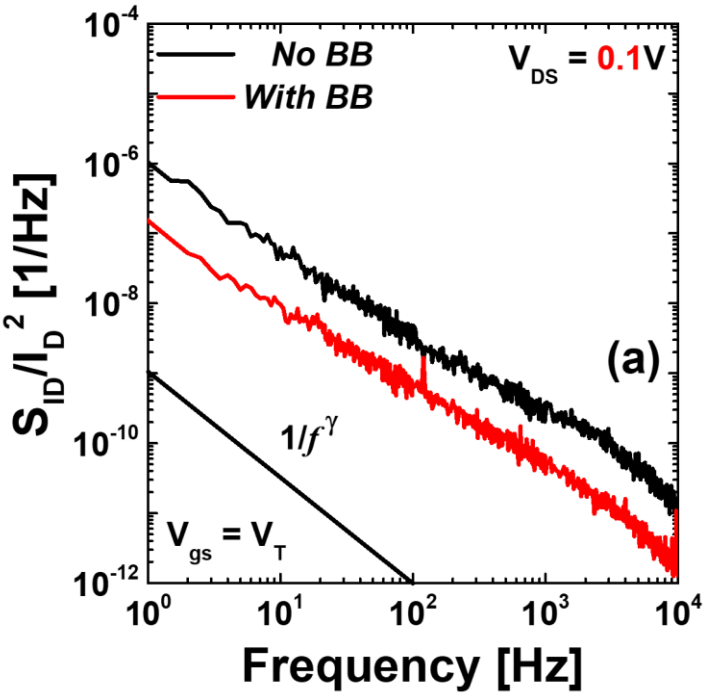



**Figure 7-6** Arrhenius plot showing $\Delta V_T$ activation energy for **(a)** $t_{ch}$ = 420 nm without back–barrier **(b)** $t_{ch}$ = 40 nm with back–barrier.

### 7.2.3 Low-Frequency Noise characteristics

Under a fixed drain bias ($V_{DS}$ = 0.1 V) and within a frequency range up to $10^4$ Hz, we performed an analysis of the 1/*f* flicker noise characteristics spanning from the subthreshold to the accumulation region. Figure 7-7 (a) presents the power-spectral density of normalized drain current ($S_{ID}/I_D^2$) for the samples at $V_{GS} = V_T$, with the frequency exponent ($\gamma$) determined by fitting the data to a $1/f^{\gamma}$ function[141]. The value of $\gamma$ was found to be close to 1 (1.1~1.2), indicating consistency in the defects/traps concerning depth and energy[134]. Notably, the $t_{ch}$ = 40 nm device exhibited lower noise density compared to the $t_{ch}$ = 420 nm device.

For quantitative trap characterization, the carrier mobility fluctuation (CMF) model was employed using the LNF data, as explained in previous chapters. A fitting curve was generated with the CMF model at a 10 Hz frequency, shown in Figure 7-7 (b) & (c). This curve provided an excellent fit with the measured data and allowed the extraction of $S_{Vfb}$ values for $t_{ch}$ = 420 nm and 40 nm, which were $1.06 \times 10^{-9}$ and $2.4 \times 10^{-11}$ $V^2 \cdot Hz^{-1}$, respectively. These $S_{Vfb}$ values were then utilized in Equation 2.16 to calculate the trap



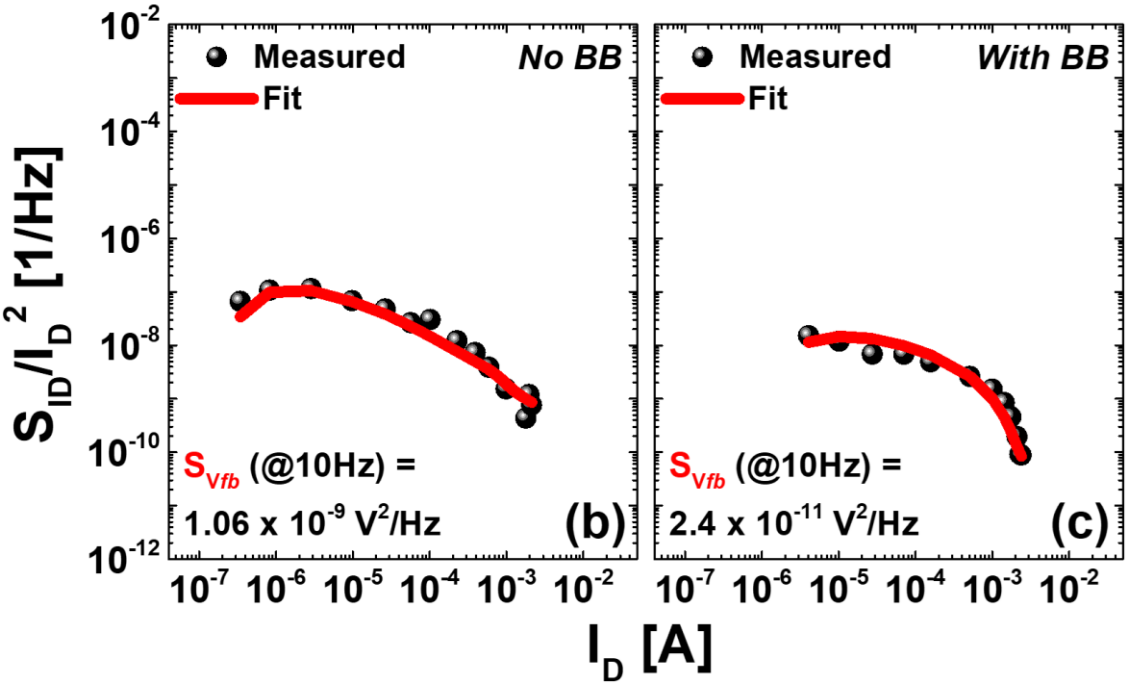



**Figure 7-7 (a)** Drain current power spectral density ($S_{ID}/I_D^2$) as a function of frequency at $V_{GS} = V_T$ and $V_{DS} = 0.1V$. Measured and modeled $S_{ID}/I_D^2$ fitting values with respect to the drain current ($I_D$) at a frequency of 10 Hz: **(a)** $t_{ch}$ = 420 nm without back–barrier **(b)** $t_{ch}$ = 40 nm with back–barrier.

density ($N_t$) of the samples. The extracted $N_t$ values were $7.1 \times 10^{19}$ and $1.7 \times 10^{18}$ $cm^{-3} \cdot eV^{-1}$ for the $t_{ch}$ = 420 nm and 40 nm devices, respectively. The inclusion of a back-barrier resulted in a reduction of over one order of magnitude in trap density in the thin channel devices.

### 7.2.4 RF Characteristics Analysis

To assess the influence of trapping on the microwave properties of the sample, we conducted RF characterizations in the frequency range of 1 to 45 GHz. A Precision Network Analyzer (PNA) system was employed for these measurements, with off-wafer calibration. To account for parasitic pad components, we used on-wafer open and short patterns for data de-embedding[135]. The measured short-circuit gain ($|h_{21}|^2$) and Mason's unilateral gain ($U_g$) for the samples were determined at $L_G$ = 80 nm under peak $g_m$ biasing conditions, as depicted in Figure 7-8 (a) & (b). By employing a least-squares fit and extrapolating the measured data with a slope of -20 dB/dec, we derived the values of $f_T$ and $f_{max}$ for the samples. For $t_{ch}$ = 420/40 nm devices, the obtained $f_T$ values were 80/120 GHz, while the $f_{max}$ values were 160/230 GHz, respectively. Figure 7-8 (c)

& (d) present the $f_T$ and $f_{max}$ values as a function of gate length $L_G$ under peak gm biasing conditions. Notably, the $t_{ch}$ = 40 nm devices exhibited a substantial enhancement in both $f_T$ and $f_{max}$, attributed to the improved transconductance ($g_m$) achieved through reduced active trapping states due to the inclusion of the back-barrier.

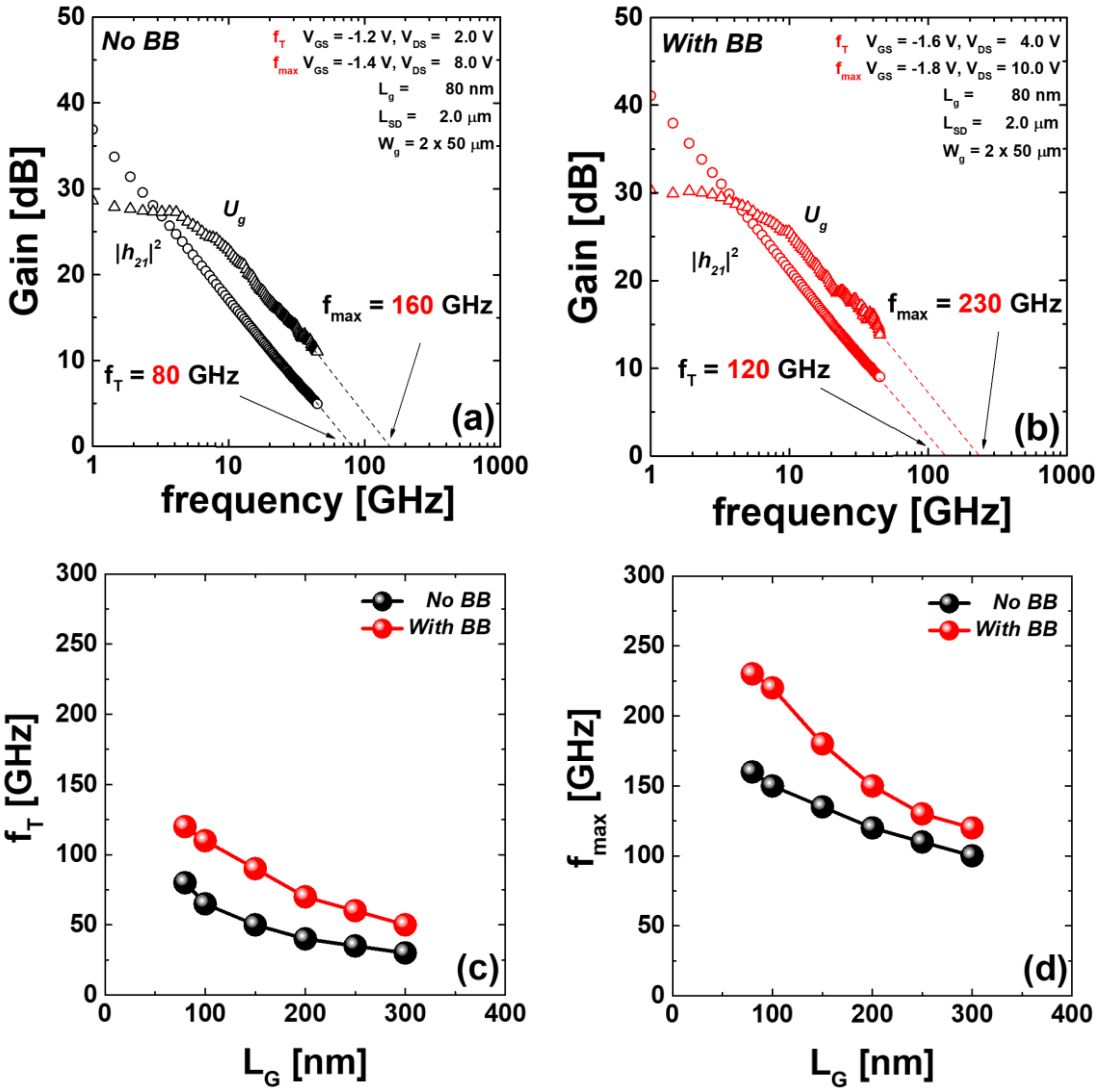



**Figure 7-8** Measured RF Gains ($|h_{21}|^2$, $U_g$) as a function of frequency, at near the peak $g_m$ bias conditions for $L_G$= 80 nm devices: **(a)** $t_{ch}$ = 420 nm without back–barrier **(b)** $t_{ch}$ = 40 nm with back–barrier. $f_T$ and $f_{max}$ values corresponding to $L_G$ for **(c)** $t_{ch}$ = 420 nm without back–barrier **(d)** $t_{ch}$ = 40 nm with back–barrier.

### 7.3 Channel thickness scaling technology

Figure 7-9 illustrates a 1-D simulation of the conduction band edge ($E_c$) and channel carrier density ($n_o$) for the samples studied in this research. Reducing the channel thickness improves the carrier density in the channel; however, it also causes the charge centroid to shift closer to the AlGaN barrier. This displacement of the channel carrier centroid towards the barrier results in stronger quantization effects, which in turn increases the likelihood of electron trapping in the AlGaN barrier[123]. In Fig. 7-10, the DC I-V characteristics of the devices are presented. The $t_{ch}$ = 40nm device exhibits noticeable higher drain current ($I_D$), transconductance ($G_m$), and on-resistance ($R_{on}$) compared to the $t_{ch}$ = 20nm device. The difference in threshold voltage between the two devices is likely attributed to variations in the interfacial trap density.

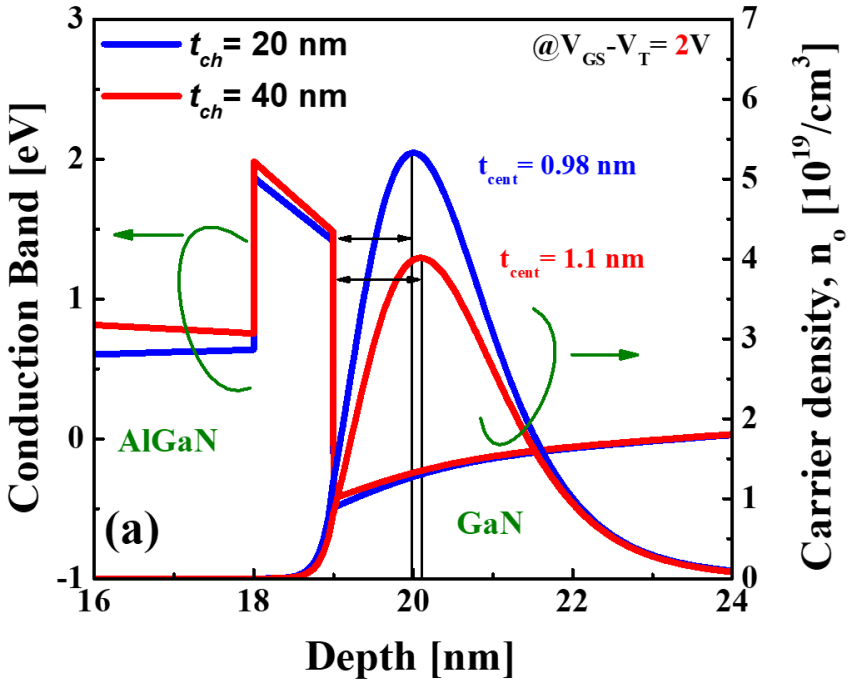



**Figure 7-9** Band ($E_c$) simulation of the samples with carrier density ($n_o$) profiles.

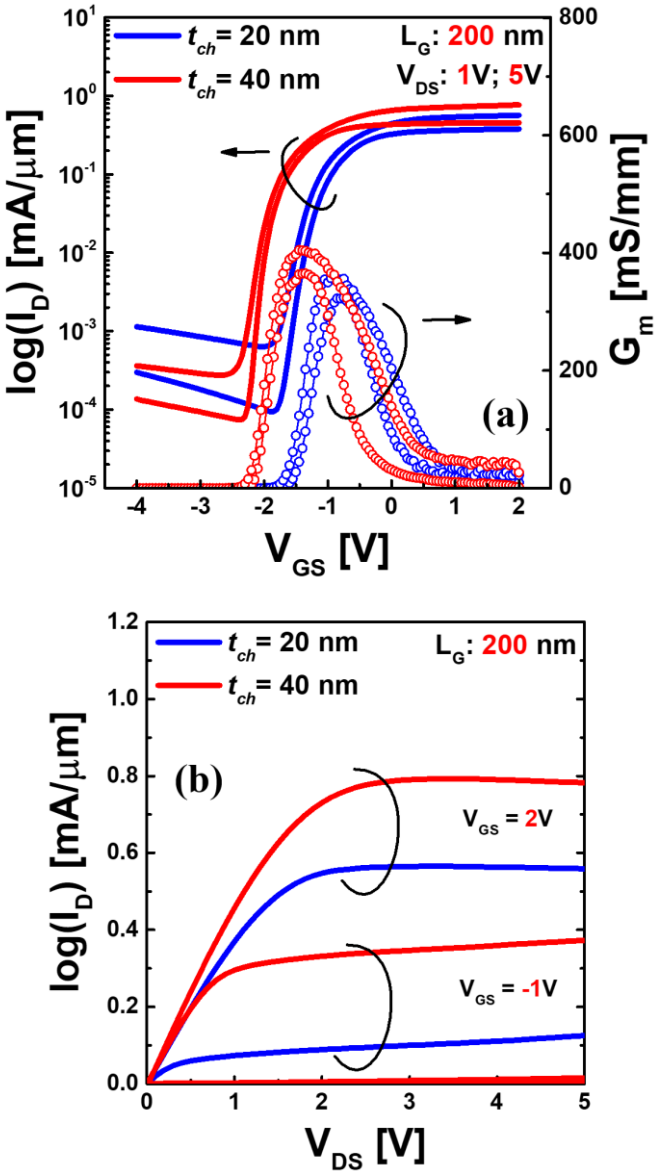



**Figure 7-10 (a)** DC transfer characteristics **(b)** Output characteristics.

### 7.3.1 PBTI Degradation and $V_T$ Shift Kinetics

PBTI stress conditions were conducted to assess the long-term reliability of the AlGaN/GaN HEMTs similar to section 7.2.2. Figure 7-11 (a) illustrates the carrier trapping and de-trapping behavior of the devices during different stress and relaxation cycles. The threshold voltage deterioration ($\Delta V_T$) observed during HCI stress is attributed to the trapping and de-trapping of electrons at defect locations inside the AlGaN barrier. The $t_{ch}$ = 40nm device shows relatively less $\Delta V_T$ compared to the $t_{ch}$ = 20nm device. Initial (1-sec stress) high $\Delta V_T$ degradation of the devices is related to the fast-transient charge trapping which is dominant over a short duration

(<1 msec) and is generated by electron tunneling from the GaN channel directly into the pre-existing shallow traps within the $Al_{0.45}Ga_{0.55}N$ layer[150]. By subtracting the fast-transient charge trapping component, a power-law expression ($\Delta V_T \sim t^n$) is used to describe the time dependence of the $V_T$ shift (Figure 7-11 (b)). The time exponent ($n$) for both devices was found to be similar ($n$ = 0.15 ~ 0.18), indicating similar interfacial degradation. However, the higher $\Delta V_T$ observed in the $t_{ch}$ = 20nm devices suggests an increased trap density inside the AlGaN barrier.

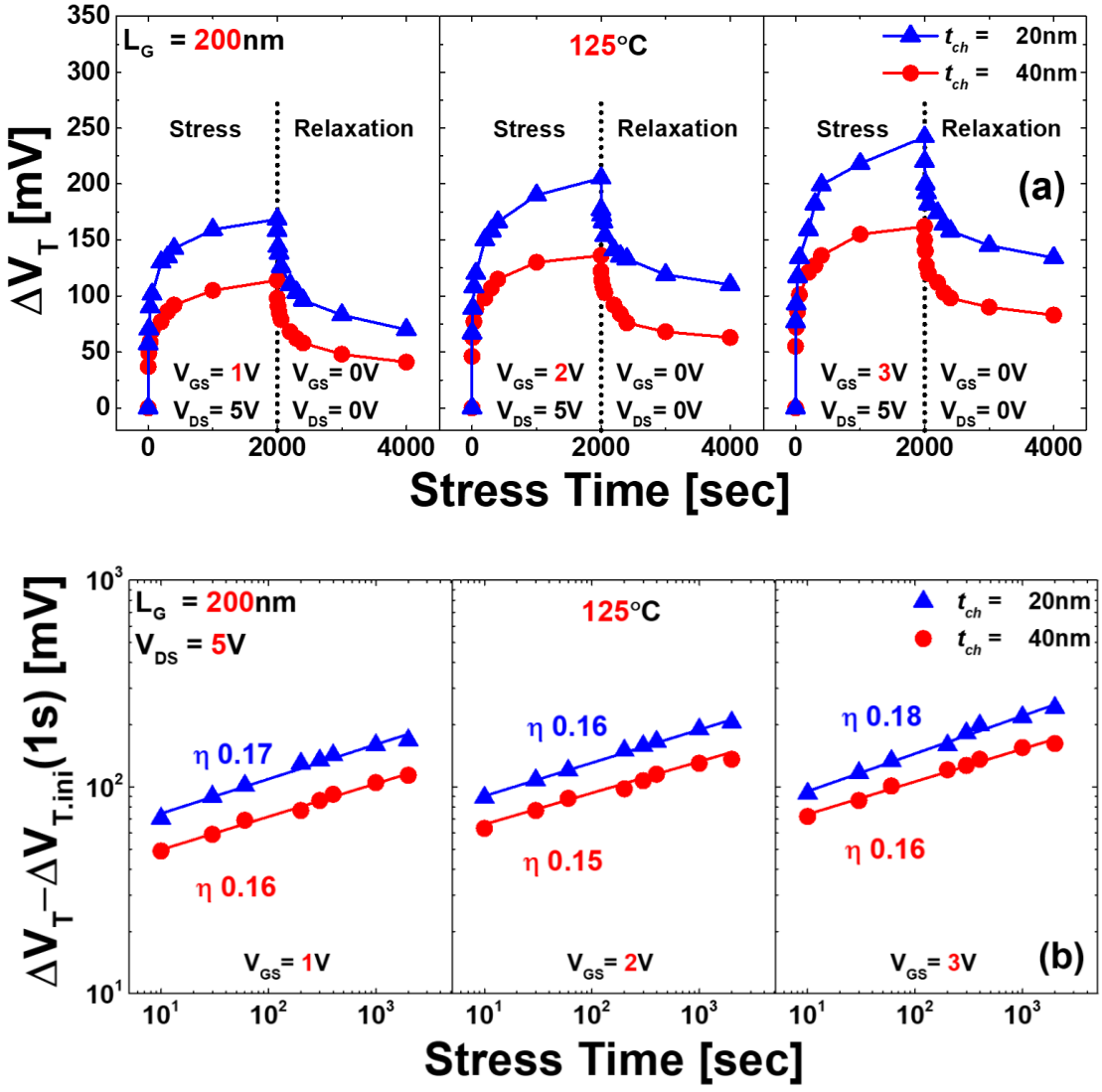
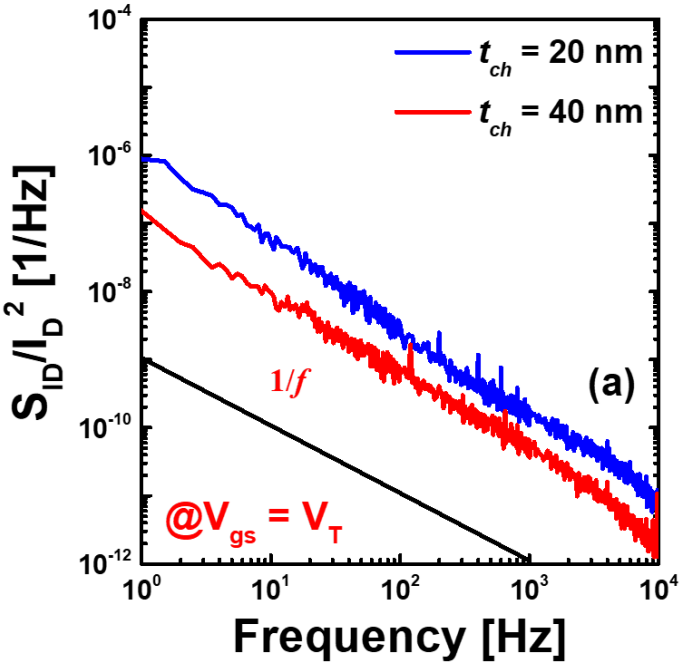



**Figure 7-11 (a)** Threshold voltage shift ($\Delta V_T$) corresponding to stress time showing charge trapping and detrapping phenomena. **(b)** Power-law time dependency of the samples after removing fast transient charging components ($V_T$ - $V_{T.initial}$ (1 s)).

### 7.3.2 Low-Frequency Noise characteristics

The 1/f low-frequency noise (LNF) characteristics were analyzed to gain insights into the trapping phenomena. By extracting the frequency exponent ($\gamma$) from the normalized drain current power-spectral density ($S_{ID}/I_D^2$) at a fixed drain bias ($V_{DS}$ = 0.5 V) and a frequency range up to $10^4$ Hz, it was found that $\gamma$ was close to 1 (1.1~1.2), indicating consistency in the defects/traps' depth and energy (Figure 7-12 (a))[133]. However, the $t_{ch}$ = 40 nm device exhibited lower noise density compared to the $t_{ch}$ = 20 nm device. For quantitative trap characterization using the LNF data, the carrier mobility fluctuation (CMF) model was employed, resulting in extracted values of $S_{Vfb}$ (at 10Hz) as 2.0 × $10^{-11}$ and 2.4 × $10^{-11}$ $V^2 \cdot Hz^{-1}$ for $t_{ch}$ = 20 nm and 40 nm devices, respectively (figure 7-13(b, c)). Utilizing these $S_{Vfb}$ values, the volume trap density ($N_t$) values were extracted as 2.8 × $10^{19}$ and 1.7 × $10^{18}$ $cm^{-3} \cdot eV^{-1}$ for the $t_{ch}$ = 20 nm and 40 nm devices, respectively. The significantly lower $N_t$ observed for the $t_{ch}$ = 40 nm devices, compared to the $t_{ch}$ = 20 nm devices, confirms the higher reliability degradation of the former.



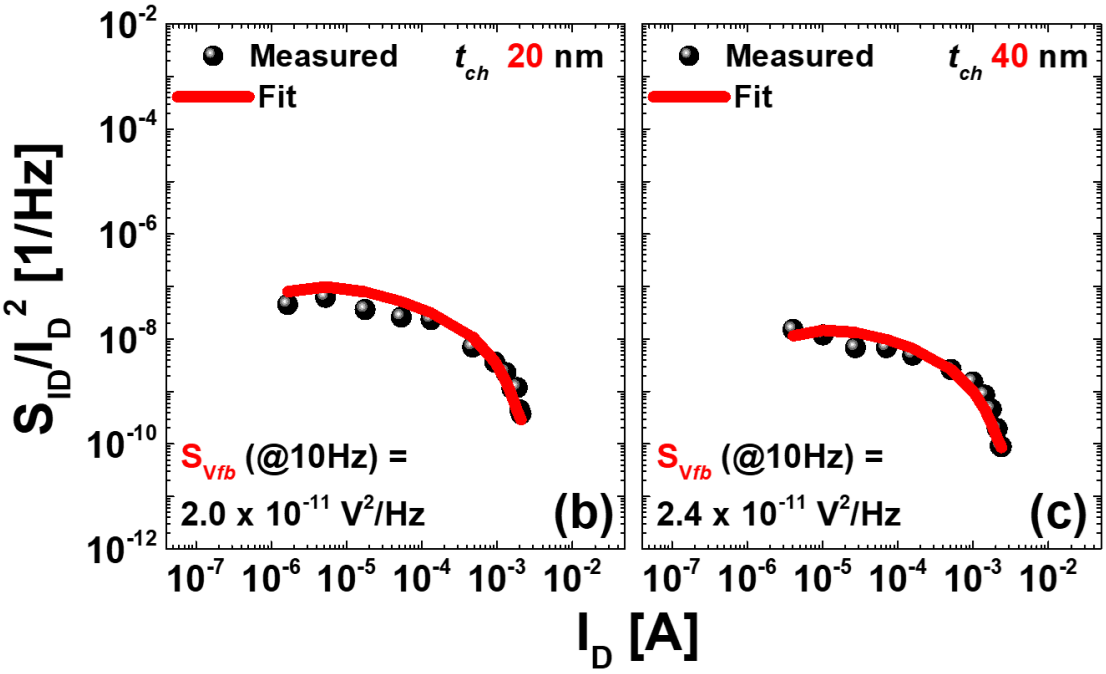



**Figure 7-12 (a)** Drain current power spectral density ($S_{ID}/I_D^2$) as a function of frequency at $V_{GS}$ = $V_T$ and $V_{DS}$ = 0.1V. Measured and modeled $S_{ID}/I_D^2$ fitting values with respect to the drain current ($I_D$) at a frequency of 10 Hz: **(a)** $t_{ch}$ = 20 nm **(b)** $t_{ch}$ = 40 nm.

### 7.3.3 RF Characteristics Analysis

To evaluate how trapping influences the microwave properties of the sample, we conducted RF characterizations spanning a frequency range of 1 to 45 GHz. Employing a Precision Network Analyzer (PNA) system with off-wafer calibration, we used on-wafer open and short patterns to compensate for parasitic pad components. Measuring the short-circuit gain ($|h_{21}|^2$) and Mason's unilateral gain ($U_g$) for the samples at $L_G$ = 80 nm under peak gm biasing conditions, as shown in Figure 7-13 (a) & (b). Using a least-squares fit and extrapolation with a slope of -20 dB/dec, we determined the $f_T$ and $f_{max}$ values for the samples. The $t_{ch}$ = 20/40 nm devices achieved $f_T$ values of 70/120 GHz and $f_{max}$ values of 110/230 GHz, respectively. Notably, the $t_{ch}$ = 40 nm devices demonstrated significant improvements in both $f_T$ and $f_{max}$ due to reduced active trapping states, resulting from a less tunnelling effect in the relatively thicker channel.

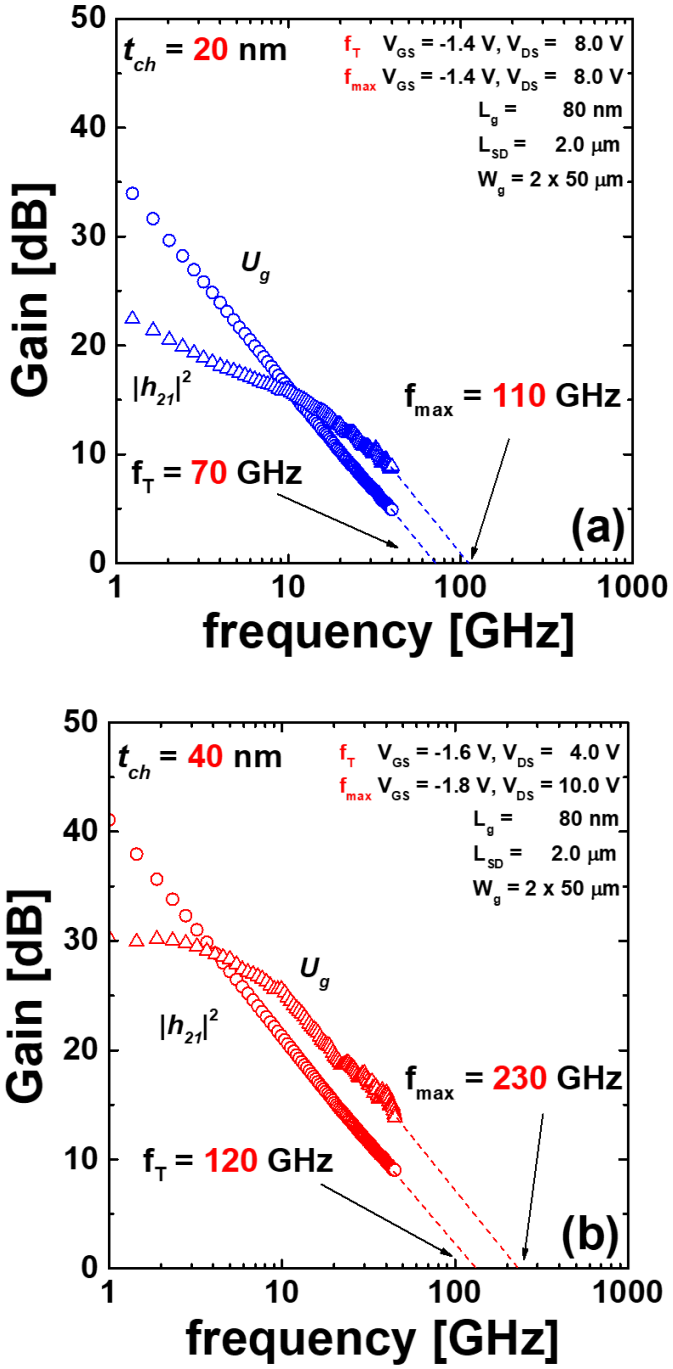



**Figure 7-13** Measured RF Gains ($|h_{21}|^2$, $U_g$) as a function of frequency, at near the peak $g_m$ bias conditions for $L_G$= 80 nm devices: **(a)** $t_{ch}$ = 20 nm **(b)** $t_{ch}$ = 40 nm.

### 7.4 Summary

In summary, our study investigated channel electron trapping within defect sites present in the barrier and buffer layer of AlGaN/GaN HEMTs. Advancements in technology often require scaling the channel thickness, which can lead to reliability issues. To tackle these challenges, we extensively explored Positive Bias Temperature Instability (PBTI) and its correlation with trapping effects, responsible for device instabilities. Our findings revealed that thick channel devices experienced a notable threshold voltage deterioration due to an increased number of trapped channel electrons in the buffer. Conversely, introducing an almost lattice-matched back barrier rectified the buffer trapping, which significantly enhances the reliability of AlGaN/GaN HEMTs, offering the potential for further channel thickness scaling. Moreover, our study demonstrated that excessive thinning of the channel results in higher tunneling of channel electrons to the barrier, contributing to device degradation. Therefore, establishing an optimal structure is crucial to enable safe scaling without compromising device performance.

# Chapter 8

# Conclusion

## 8.1 Summary

In this thesis, we investigated the physics of trapping-related degradation in AlGaN/GaN high electron mobility transistors. This work is a follow-up to our previous research, focusing on investigating various fundamental degradation mechanisms stemming from different structural issues[10][151][133][150]. We conducted in-depth reliability characterizations and trap extractions to modify the epi-structure of AlGaN/GaN HEMTs, aiming to enhance device reliability and performance. Establishing a systematic relationship between trapping effects and device performance, we endeavored to mitigate various types of trapping effects, especially hot electron effects, by modifying the structure to improve device performance.

Firstly, we focused on trapping effects in the AlGaN barrier and AlGaN/GaN interface and proposed using frequency-dependent C-V and G-V methods to extract the interfacial trap densities ($D_{it}$, $N_{bt}$) in previous work[10]. For the first time, we utilized conventional frequency-dependent C-V and G-V methods to characterize the interface trap density ($D_{it}$) between AlGaN and GaN layer, and the deep-level/border trap density ($N_{bt}$) in the AlGaN barrier layer of a long-channel AlGaN/GaN HEMT constructed on a SiC substrate. Normally, these frequency-dependent C-V and G-V methods are employed to analyze the trapping characteristics of dielectrics/oxides in a MOS structure. Yet, we applied these methods to our device structure due to the AlGaN barrier layer possessing a wide band gap of approximately ~4 eV and a high dielectric constant of about ~9.4, causing it to function similarly to an insulator, resembling a dielectric material. Our primary focus was on the trap states within the AlGaN layer, particularly located at or near the interface of the AlGaN/GaN, while striving to eliminate other potential interfacial trap-contributing factors, such as dielectric layers used for passivation. Through the use of conventional frequency-dependent C-V and G-V characteristics, we sought to comprehend

the interactions of the interface traps. Additionally, we delved into the deep-level/border trap behavior in the accumulation region by scrutinizing split C-V characteristics, commonly observed in conventional Si MOS structures. While certain researchers have explored methods like threshold voltage shift profiling and discharging-based trap energy profile techniques for border/bulk trap extraction, the frequency-dependent C-V method for border trap density extraction in the AlGaN/GaN heterostructure has not been presented. Unlike prior studies concentrating mainly on insulator/AlGaN interface trap extraction, our aim was to explore the AlGaN/GaN interface for this purpose. We ensured the validity of the extracted $D_{it}$ and $N_{bt}$ values by comparing them with theoretical and experimental calculations as well as values of similar structures from the literature.

Next, we investigated the impacts of the Al composition in the $Al_xGa_{1-x}N$ barrier on device performance by assessing reliability across two distinct $Al_xGa_{1-x}N$ /GaN HEMTs [x = 0.25, 0.45]. Single-pulse $I_D$-$V_D$ characterization revealed higher drain-current degradation ($\Delta I_D$) over time in $Al_{0.45}Ga_{0.55}N$/GaN devices, attributable to fast-transient charge trapping near the $Al_xGa_{1-x}N$/GaN interface. Constant voltage stress (CVS) measurements supported this, showing higher threshold voltage shifting ($\Delta V_T$) due to stress electric fields, confirming higher interfacial deterioration in $Al_{0.45}Ga_{0.55}N$/GaN devices. In contrast, the $Al_{0.25}Ga_{0.75}N$/GaN device displayed a substantial 35% reduction in interface trap density ($D_{it}$) and a remarkable 73% decrease in border trap density ($N_{bt}$), signifying reduced trapping in comparison to $Al_{0.45}Ga_{0.55}N$/GaN. The extraction of volume trap density ($N_t$) using low-frequency noise characterizations underscored a 40% reduction in $N_t$ for $Al_{0.25}Ga_{0.75}N$/GaN, affirming the higher trapping phenomenon in $Al_{0.45}Ga_{0.55}N$/GaN due to a rougher interface. The study highlighted the tunneling probability of channel electrons through the barrier, noting an increased Al composition leading to reduced tunneling distance and making the devices more vulnerable to hot carrier degradation. The defect sites in the $Al_xGa_{1-x}N$ barrier and $Al_xGa_{1-x}N$/GaN interface were recognized as the primary causes of transient-charging effects. This charging follows two processes: fast and slow transient charging. The fast process impacts mobility degradation and threshold voltage ($V_T$) instability, while the slow process causes long-term $V_T$ instability. Though $Al_{0.25}Ga_{0.75}N$/GaN devices showed better reliability compared to the $Al_{0.45}Ga_{0.55}N$/GaN devices, they were limited in microwave RF performances due to reduced 2DEG concentration. This analysis emphasized the importance of analyzing these trapping effects for the reliability of $Al_xGa_{1-x}N$/GaN HEMTs. Furthermore, the impact of reduced Al content on carrier transport, transconductance, and RF performance in GaN-based devices was

analyzed, leading to considerations for future works exploring means to enhance device quality while maintaining high-performance metrics.

Further, a comprehensive analysis of the volume and surface-related trapping phenomena is presented, focusing on their impact on RF transconductance ($g_m$) compared to DC transconductance ($G_m$). To address this, $O_2$ plasma treatment was applied before the deposition of the gate metal onto an AlGaN layer, targeting improvements in both bulk and surface trapping states. This analysis illustrates the profound impact of $O_2$ plasma treatment on volume trap states within the AlGaN barrier layer of an AlGaN/GaN HEMT, showcasing significant enhancements in device performance. Analytical techniques such as X-ray Photoelectron Spectroscopy (XPS) and High-Resolution X-ray Diffraction (HR-XRD) were employed to assess the bulk effects of the $O_2$ plasma treatment. The $O_2$ ions effectively passivated the AlGaN gate surface and extended their influence into the bulk, forming crucial Al–O and Ga–O bonds that addressed volume trap states. Results clearly demonstrate the superior Schottky characteristics of the $O_2$ plasma-treated sample compared to the as-grown sample, with the former maintaining a stable drain current under reverse-sweep drain-stress bias conditions, in contrast to the drain current collapse in the as-grown sample. Moreover, single-pulse and 1/*f* noise characterizations confirmed a remarkable 67% reduction in volume trap states due to the plasma treatment, resulting in significantly improved values for $f_T$ and $f_{max}$. Furthermore, load-pull analysis highlighted substantial enhancements in $P_{out\_max}$, Power Added Efficiency (PAE), and linear gain. The power output increased from 1.25 W/mm to 2.4 W/mm, PAE improved from 20% to 50%, and linear gain rose from 15 dB to 19 dB for the $O_2$ plasma-treated sample. The work delves into the intricacies of addressing and improving Hot Electron Degradation, further enhancing the understanding of HEMT performance.

Finally, we did a comprehensive investigation into Positive-Bias-Temperature Instability (PBTI) and hot electron trapping behaviors in AlGaN/GaN HEMTs, particularly emphasizing the impact of aggressive scaling down of the channel thickness. Our study utilized AlGaN/GaN HEMTs with minor differences in design, focusing on varying channel thickness and the inclusion of an $Al_{0.08}Ga_{0.92}N$ channel back barrier. Devices underwent extensive long-term reliability testing under high drain bias and elevated ambient temperatures to analyze trapping phenomena. Pulsed I-V and low-frequency 1/*f* noise characterizations were performed to quantitatively estimate trap densities. Additionally, Scattering parameter (S-parameter) measurements were conducted to assess how these trapping phenomena affected the microwave

characteristics of the devices. This work consists of two primary sections: initially investigating the impact of introducing the $Al_{0.08}Ga_{0.92}N$ channel back barrier to mitigate "Hot electron effects" in the buffer. Subsequently, it delves into exploring how the scaling of the channel thickness influences these hot electron effects. This study examined channel electron trapping within defect sites found in the barrier and buffer layer of AlGaN/GaN HEMTs. Technological advancements often necessitate scaling the channel thickness, leading to potential reliability issues. The research extensively explored Positive Bias Temperature Instability (PBTI) and its correlation with trapping effects, highlighting the thick channel devices' notable threshold voltage deterioration due to an increased number of trapped channel electrons in the buffer. Conversely, introducing an almost lattice-matched back barrier rectified the buffer trapping, significantly enhancing the reliability of AlGaN/GaN HEMTs, and potentially allowing for further channel thickness scaling. Furthermore, the study revealed that excessive thinning of the channel results in increased tunneling of channel electrons to the barrier, leading to device degradation. Therefore, establishing an optimal structure is crucial for enabling safe scaling without compromising device performance.

## 8.2 Recommendations for enhancing device performance & maintaining reliability

The physical understanding of the trapping or degradation mechanism that involves the hot electron effect suggests several solutions to its mitigation or elimination. As is often the case, these approaches normally entail drawbacks, and most often there is a tradeoff between performance and reliability.

Since the degradation mechanism that we postulate occurs when the hot electrons are trapped in the AlGaN surface, barrier and buffer layer under the device operating conditions, one of the most efficient ways to reduce these effects should be to use a proper passivation layer for the AlGaN barrier. As there is no such good native oxide of AlGaN for the passivation layer, we often use $SiN_x$, $Al_2O_3$, $SiO_2$ etc. The passivation layers actively passivate the surface traps and can significantly increase the device breakdown voltages as well as output power. Plasma treating the AlGaN surface also helps to passivate the surface traps as well as the volume traps inside the AlGaN layer which we already showed in our work. These passivation techniques will enhance the overall reliability under high electric field stresses and the longevity of the HEMTs will be ensured.

The introduction of the GaN cap layer may serve to diminish gate leakage current by mitigating both the tunneling and thermionic emission components associated with it. Additionally, this GaN cap layer plays a role in passivating surface states, thereby decreasing the surface leakage current that occurs between the gate and the drain[152].

Another path to mitigation of hot electron effects in the buffer layer should be the use of channel back barriers. Channel back barriers are highly resistive and cause hot electrons not to pass through into the buffer layer. It also improves the carrier confinement in the channel and improves carrier transport.

### 8.3 Suggestions for future work

While we have conducted thorough investigations into the physics of electrical degradation in GaN HEMTs, numerous unresolved issues persist, demanding a comprehensive understanding for the enhancement of device reliability. In this segment, we propose key areas for future research that demand further analysis.

As outlined in this thesis, our experimental findings align predominantly with the defect formation mechanism induced by trapping and hot electron effects. Nevertheless, additional experiments are necessary to enhance the understanding and validation of our hypothesis. Primarily, investigating the characteristics of high-frequency noise becomes imperative. Our current experimental setup lacked the capability to characterize high-frequency noise due to insufficient device setup. A comprehensive analysis of s-parameter characteristics, incorporating the effects influenced by temperature-dependent Rs and Rd, would be beneficial. The insights gained from this analysis could serve as a valuable reference for the design of low-frequency GaN LNAs and, more specifically, millimeter-wave GaN LNA-PA designs, particularly when applied under varying ambient temperatures.

From a theoretical standpoint, the $O_2$ plasma treatment outlined in Chapter 6, conducted before gate deposition, warrants further extension. Our current investigation has focused solely on passivating surface and bulk defect states within the gate region, resulting in enhanced device performance. However, there is a potential for additional performance improvements by extending the plasma treatment to cover the entire AlGaN surface, spanning from source to drain. This broader treatment approach is anticipated to effectively passivate surface states in the access region, potentially leading to a more significant performance boost.

To enhance carrier confinement in the GaN channel and mitigate hot electron trapping in the buffer, we incorporated a 400nm thick $Al_{0.08}Ga_{0.92}N$ back barrier. However, there is potential for further exploration in back-barrier technology. Multi-layer back barrier can be a promising technology. In a multi-layer back-barrier, Al composition gradually increases from the channel layer to the substrate layer, remaining consistent within each back-barrier layer. This structural configuration can reduce the peak value of the channel electric field, effectively modulating the channel electric field and augmenting the device's breakdown voltage. In comparison to field

plate technology, the multi-layer back-barrier structure will not significantly increase the gate capacitance, thereby exerting minimal influence on the frequency characteristics of the device. Moreover, when compared to a single-layer back-barrier structure, the multi-layer back-barrier design can leverage multiple low-component back barriers to collectively regulate the channel electric field without introducing a two-dimensional hole gas (2DHG). This approach can effectively increase the device's voltage withstand capability while maintaining a higher device saturation current.

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# 초고주파 장치를 위한 GaN 기반 고전자 이동도 트랜지스터의 최적화: 성능 및 신뢰성 향상에 관한 종합적 연구

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**요약**

고주파 및 고출력 응용 분야에서 GaN 기반의 고전자 이동성 트랜지스터 (HEMT)의 광범위한 적용은 여전히 낮은 신뢰성 문제를 안고 있습니다. 이러한 신뢰성을 향상시키는 것은 GaN HEMTs 소자의 높은 구동 전압과 GaN 의 물질적 특성으로 인해 도전적인 과제로, 주로 어떤 요소가 이러한 신뢰성 저하를 일으키는지에 대한 물리적인 현상의 이해가 가장 중요한 요소로 간주됩니다. 위 논문은 AlGaN/GaN 고전자 이동성 트랜지스터 (HEMT)의 Trapping 관련 성능 저하에 대한 심층적인 연구를 통해 에피 구조적 문제에 대한 선행 연구를 개선했습니다. 주파수 의존적 C-V 및 G-V 방법을 사용하여 계면과 경계 trap 을 철저히 특성화하고, 다각적인 측면에서 소자의 trap 현상을 연구했으며, AlGaN 장벽의 Al 몰분율이 소자의 성능에 미치는 영향을 관찰하여 트랩 밀도와 그 결과에 대한 물리적 의미를 밝혔습니다. 소자의 Volume trap state 를 완화하기 위한 O2 플라즈마 처리를 통한 쇼트키 특성 및 마이크로파 성능의 개선을 확인하였으며, PBTI (Positive-Bias-Temperature Instability)와 채널 back barrier 및 채널 두께 스케일링에 따른 신뢰성 특성에 대한 분석을 통해 다양한 구조적 요인과 trap 현상에 대한 복잡한 상관관계를 규명했습니다. 전반적으로 위 연구는 AlGaN/GaN HEMT 의 Trapping effect 에 대한 물리적 이해를 통해 다양한 작동 조건에서의 소자의 신뢰성과 성능을 향상시키기 위한 GaN HEMTs 의 구조를 제안합니다.