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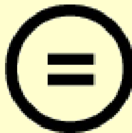

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Doctor of Philosophy

Reliability Assessment and Degradation Physics of AlGaN/GaN HEMTs

The Graduate School
of the University of Ulsan

Department of Electrical, Electronic and Computer Engineering

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Reliability Assessment and Degradation Physics of AlGaN/GaN HEMTs

Supervisor: Sunghwan Kim

A Dissertation

Submitted to
the Graduate School of the University of Ulsan
In partial Fulfillment of the Requirements
for the Degree of

Doctor of Philosophy
by

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February 2024

Reliability Assessment and Degradation Physics of AlGaN/GaN HEMTs

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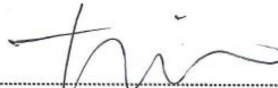

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Reliability Assessment and Degradation Physics of AlGaN/GaN HEMTs

by

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ABSTRACT

The widespread adoption of Gallium Nitride High-Electron-Mobility Transistor (GaN HEMT) technology has faced significant challenges, primarily related to its electrical reliability. While GaN HEMTs demonstrate remarkable resilience against a range of electrical overstress conditions, guaranteeing their long-term reliability has emerged as a critical concern. The pivotal parameter for evaluating device longevity, the Mean Time To Failure (MTTF), has often eluded precise estimation, despite extensive long-term reliability tests conducted under varying temperature conditions. This doctoral thesis undertakes a comprehensive exploration of the profound impact of electrical field stress on long-term reliability, with a particular focus on GaN HEMTs. It delves deep into the intricate physical mechanisms underpinning device degradation, with a primary focus on the effects of hot electron-induced trap phenomena and impact ionization. Emphasizing that MTTF values are influenced not only by temperature but also by the specific electric field stress conditions, this research seeks to provide a profound understanding of these degradation mechanisms and their broader implications. This understanding lays the groundwork for the intentional design of device structures that optimize both performance and reliability. To unravel these intricate complexities, a systematic analysis of the degradation of critical parameters in GaN HEMTs, including drain current (I_{DS}), threshold voltage shift (ΔV_T), transconductance (G_{MAX}), on-resistance (R_{ON}), and gate leakage current (I_{g_leak}) under various bias

conditions within the High-Temperature Operating Life (HTOL) test, is conducted. The unique proposition of a combined acceleration factor that considers both voltage and temperature facilitate precise MTTF determination, recognizing that AlGaN/GaN HEMTs exhibit a complex interplay between electric field/voltage and temperature for reliability. Finally, an in-depth analysis of three distinct HEMT technologies, including hot electron and hot electron-induced impact ionization, reveals that these mechanisms are predominant during On-stress testing and contribute significantly to electrical degradation.

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Chapter 1

Introduction

1.1 Wide band Gap Semiconductors

Wide bandgap (WBG) semiconductors constitute the forefront of materials meeting these stipulations, encompassing material families such as group IV, III–V, and II–VI. Examples within these families include silicon carbide (SiC) with a bandgap energy of 3.2 eV, gallium nitride (GaN) with a bandgap energy of 3.4 eV, and zinc oxide (ZnO) with a bandgap energy of 3.4 eV, respectively [1]. Ultrawide bandgap (UWBG) semiconductors, characterized by bandgap energies surpassing 4 eV, encompass a select group of materials. Noteworthy examples within this category comprise diamond, III-nitrides doped with aluminum and boron (e.g., AlN, BN, and AlGaN), as well as sesquioxides such as Ga_2O_3 and $(Al,Ga)_2O_3$. These materials encompass a spectrum of technological readiness, where SiC and GaN platforms stand as some of the most mature, featuring readily available commercial devices in the domains of radio frequency (RF) and high-power electronics. Conversely, platforms like Ga_2O_3 are experiencing rapid advancements and are positioned to facilitate the development of novel ultraviolet (UV) and deep-ultraviolet (deep-UV) optoelectronic devices.

In the realm of high-voltage and high-power applications, specifically within the lower frequency spectrum, certain materials encounter inherent limitations. Consequently, alternative materials possessing greater bandgap and breakdown voltage characteristics, such as GaN and SiC, are employed in these scenarios [2]. SiC has a large bandgap of 3 eV and much higher thermal conductivity compared to Si. [3]. The high bandgap of SiC allow operation as a semiconductor up to temperatures 1000°C, while Si becomes intrinsic above roughly 400°C. [4] Silicon carbide (SiC) MOSFETs are exceptionally well-suited for high-power applications with demanding breakdown voltage requirements, particularly in high-frequency operation. By contrast, optoelectronics is the major market for GaN [5]. Nonetheless, both SiC and GaN exhibit

material characteristics that bear similarities to those of conventional silicon and the exceptional semiconductor material, diamond shown in the table 1.1 [6].

Table 1.1 Material properties of SiC and GaN in comparison with Silicon and Diamond

Parameter	Silicon	4H-SiC	GaN	Diamond
W_g [eV]	1.12	3.26	3.39	5.47
E_{crit} [MV/cm]	0.23	2.2	3.3	5.6
ϵ_r	11.8	9.7	9.0	5.7
μ_n [$cm^2/V.s$]	1400	950	800/1700[2]	1800
BFoM relative to Si	1	500	1300/2700[2]	9000
n_i [cm^{-3}]	1.10^{10}	8.10^{-9}	2.10^{-10}	1.10^{-20}
λ [W/cm.K]	1.5	3.8	1.3/3[3]	20

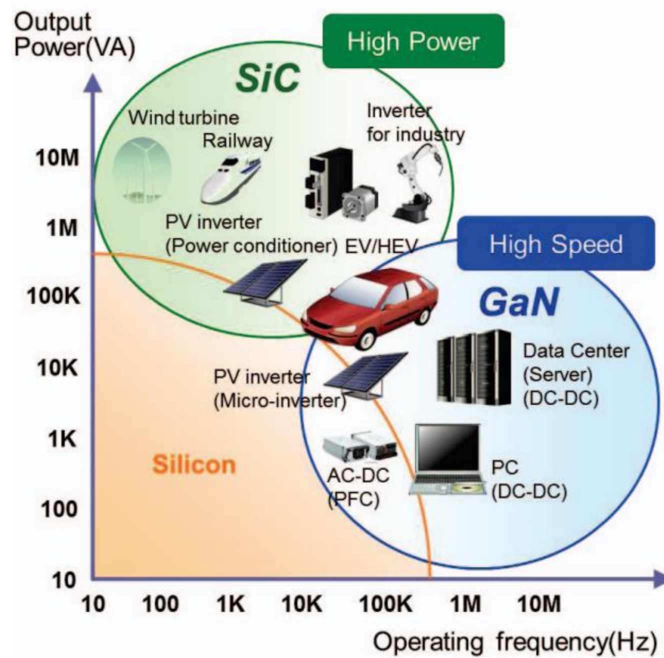


Figure 1.1 : Wide bandgap semiconductors are being applied in advanced electronic devices for consumer use, electric vehicle charging, telecommunications, switch-mode power supplies, solar energy systems, industrial battery formation, and automotive onboard charging, as well as high-voltage to low-voltage DC-DC converters.

Across the majority of parameters, gallium nitride (GaN) demonstrates a slight superiority over silicon carbide (SiC), notably yielding a threefold increase in Baliga's Figure of Merit (FoM) for power devices [7]. Fig 1 shows the future markets of the wide bandgap semiconductors which are shared by SiC and GaN. In evaluating GaN HEMTs for high-power applications, it is crucial to consider the device-level breakdown characteristics. The enhancement of the breakdown voltage in GaN transistors is presently constrained to approximately 2200 V due to the limitations of the GaN epilayer thickness (3.2 μm). [8]. specifically, a comprehensive understanding and establishment of reliability are imperative prerequisites to expand the market presence of these promising wide bandgap semiconductors.

1.2 Introduction to GaN HEMTs

Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) hold significant promise for applications requiring high voltage switching and high-power RF capabilities, owing to a myriad of distinctive material attributes inherent to GaN technology. GaN based transistors display highly advantageous characteristics for high-frequency power applications, primarily attributable to their substantial band gap of 3.4 eV, exceptional breakdown field of approximately 3.5 MV/cm, low on-state resistance, and effective thermal management capabilities [9-13]. In the absence of doping, the AlGaN/GaN heterostructure demonstrates a significant conduction band discontinuity. This, when coupled with the influences of piezoelectric polarization and spontaneous polarization, gives rise to the creation of a high-density two-dimensional electron gas (2-DEG) [14-16]. Furthermore, owing to the substantial conduction band discontinuity observed between AlGaN and GaN, the AlGaN/GaN structural configuration exhibits a notably elevated electron mobility exceeding 1500 cm^2/Vs and an impressive electron saturation velocity of 2.5×10^7 cm/s [17]. This capability facilitates the attainment of high-frequency and high-power operational characteristics, as evidenced by the successful demonstration of an f_T (unity current gain cutoff frequency) reaching 250 GHz and f_{max} of 204 GHz through the utilization of a device featuring a 55 nm gate length (L_g) using T-gate and n^{++} -GaN source/drain contacts [18]

Thanks to these exceptional material properties inherent to GaN, AlGaN/GaN High Electron Mobility Transistors (HEMTs) have exhibited remarkable performance across a broad spectrum of frequencies within the realm of RF power applications. The latest breakthrough of GaN HEMTs (first four finger 4 x 25 μm) was recorded output power density 7.1 W/mm with 31.7% power added efficiency (PAE) in W band (94 GHz) range [19]. The power densities achieved by these devices surpass conventional technologies based on GaAs or InP by an order of magnitude, underscoring their superior performance in this regard. Reliability of AlGaN/GaN HEMTs has

been improved for using wireless base station by implanting n-GaN cap layer which also includes breakdown voltage around 1600 V [20].

1.3 Basic Principles of GaN HEMTs

The potential of heterostructure technology is a significant advantage of III-V nitrides in comparison to SiC. This technology allows for the creation of structures such as quantum wells, modulation-doped structures on piezoelectric heterointerfaces, and heterojunctions. These capabilities open up new spectral regions for optical devices and enable novel operating regimes for electronic devices. In this regard, III-V nitrides can be viewed as the wide bandgap equivalent of the AlGaAs/InGaAs system, which has established a contemporary standard for microwave device performance [21].

In AlGaN/GaN HEMTs, a conductive channel is formed at the heterointerface, and this channel is characterized by a Two-Dimensional Electron Gas (2DEG). The significant advantage of a 2DEG channel is the ability to enhance conductivity by increasing carrier concentration without experiencing the mobility degradation caused by impurity scattering. To experimentally confirm the presence of a 2DEG, one can assess the temperature-dependent carrier mobility and carrier concentrations through low-temperature Hall measurements [21].

The AlGaN/GaN HEMTs is a three-terminal device that can be characterized by its gate length (L_G), gate width (W_G), and the distances between the Source and Gate (L_{SG}) and between the Source and Drain (L_{SD}). Electron transport in the 2DEG occurs between the ohmic contacts of the Drain and Source. The flow of current is controlled and modulated by the bias applied to the gate Schottky contact (Figure 1.2). Applying a negative bias to the gate and the source electrode reduces the positive charge density near the metal-semiconductor interface, depleting the 2DEG. Complete pinch-off of the channel can be achieved by increasing the negative voltage V_G to $V_{GS} = V_{TH}$ (threshold voltage).

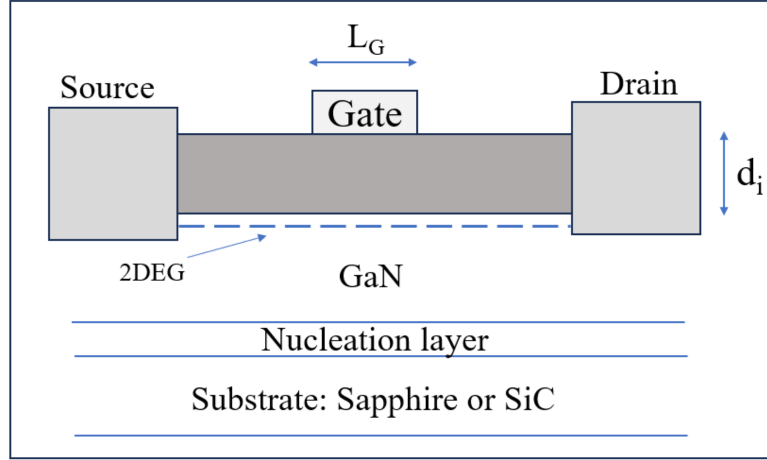


Figure 1.2: A **typical AlGaN/GaN HEMT structure**

The dependence of the 2DEG sheet carrier concentration (n_s) on the applied gate-source voltage (V_{GS}) at small drain-source biases can be expressed by the following equation:

$$n_s = \frac{\varepsilon\left(V_{GS} - V_{th}\right)}{q\left(d_i + \Delta d\right)} \tag{1.1}$$

Where, V_{th} represents threshold voltage , d_i = thickness of AlGaN, ϵ= dielectric permittivity of AlGaN, Δd = effective thickness of the 2DEG.

In equation above equation, the threshold voltage is defined as the gate voltage at which the conductance of the channel drops to zero:

$$V_{th} = \Phi_b - V_P - \frac{\Delta E_c}{q} \tag{1.2}$$

Where, ϕ_b = Schottky barrier height, V_p = pinch-off voltage, ΔE_c = heterojunction discontinuity.

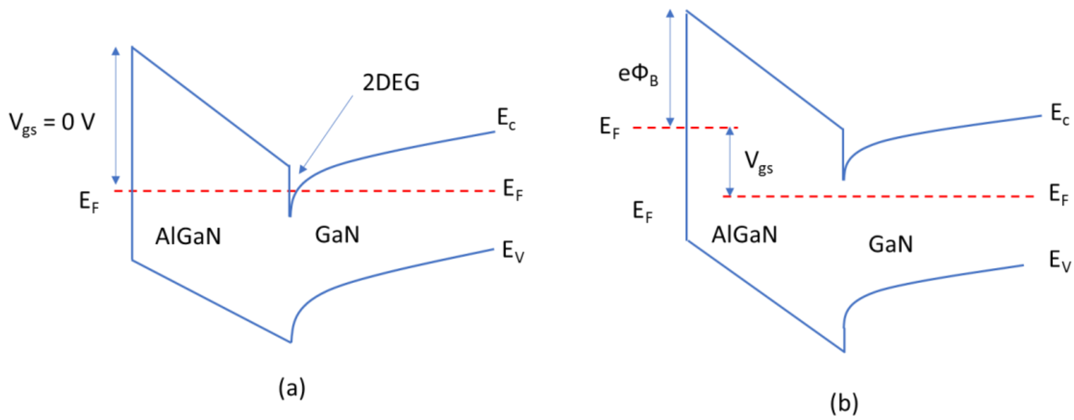


Figure 1.3: **Band diagram of AlGaN/GaN HEMT in equilibrium and (b) after negative biasing of the gate.**

The drift current at any point along the channel is given by:

$$I(x) = W_g \mu_0 q n_s E(x) \quad (1.3)$$

Where, μ_0 is low electric field mobility and $E(x)$ the electric field along the channel. The output characteristics of the GaN HEMTs are shown in Figure 1.4:

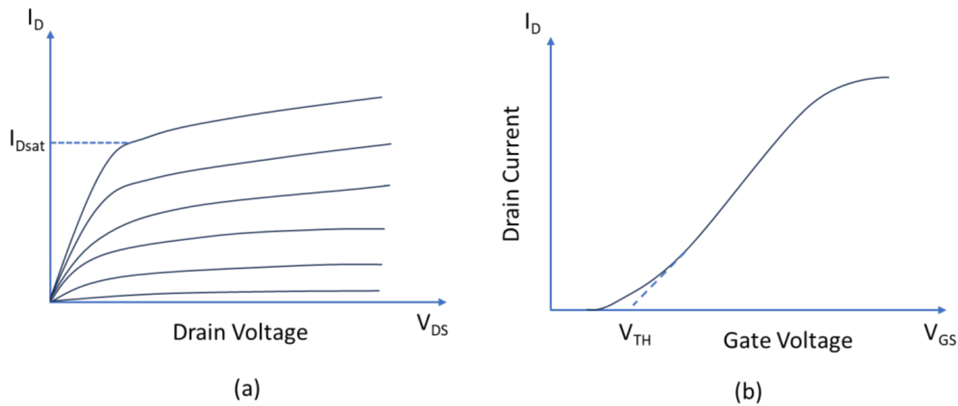


Figure 1.4: (a) Output Characteristics and (b) Transfer Characteristics of an GaN HEMT

As is typical for FET transistors, the output characteristic can be divided into an ohmic (linear) region and a saturation region. The ohmic region is defined by the following equation:

When $V_{DS} << (V_{GS} - V_{th})$, the current equation can be written as

$$I_{DS_LIN} = \mu_0 c_0 \frac{W_g}{L_{DS}} \left(V_{GS} - V_{th}\right) V_{DS} \tag{1.4}$$

Where $c_0 = \epsilon/(d_i+\Delta d)$ and for the saturation current, it can be expressed by

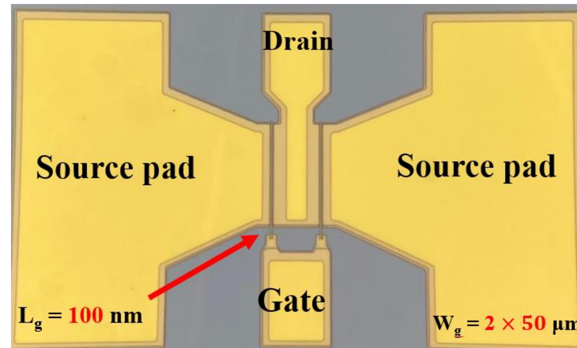
$$I_{DS_SAT} = \frac{W_G \mu_0 c_0}{2L_{DS}} (V_{GS} - V_{th})^2 \tag{1.5}$$

The breakdown voltage is defined as the drain-source voltage at which the electric field in the material reaches the critical value Ec, and the breakdown of the gate-drain junction begins. An increase in junction current can raise the temperature in the material, potentially leading to transistor burnout unless a safe working region is clearly defined.

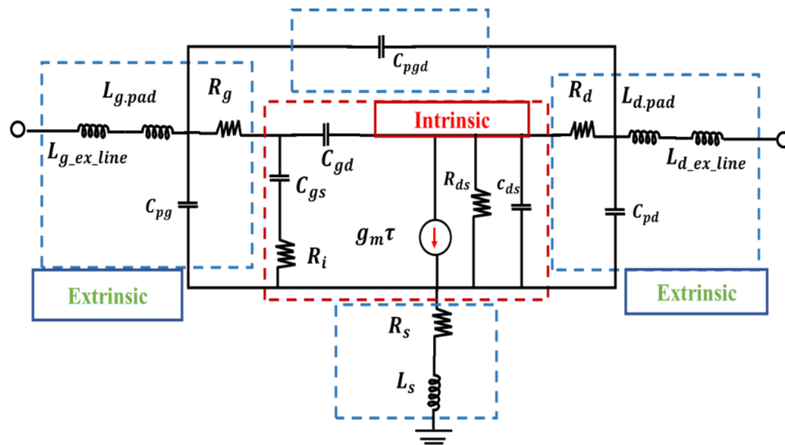
1.3.1 Small Signal Model and Parasitic Components of RF AlGaN/GaN HEMTs

The utilization of the small-signal model for a High Electron Mobility Transistor (HEMT) facilitates the assessment of device parameters, enabling a comprehensive analysis of its small-signal characteristics across varying frequencies. It is widely assumed that an appropriate extraction technique for a robust small-signal equivalent circuit is critical for circuit design, process technology assessment, and device performance optimization [22, 23]. The important characteristics of AlGaN/GaN HEMTs are high sheet carrier density ($n_s >> 1 \times 10^{13}$ cm^{-2}) that produces high I_{max}, mobility of electron is high ($\mu > 1500$ cm^2/V$_s$) which suitable for low on-resistance (R_{on}), high breakdown voltage and high operating channel temperature. [24, 25, 26]. Several groups have investigated the high-performance DC analysis of AlGaN/GaN HEMTs [27, 28]. Nonetheless, the theoretical studies of AlGaN/GaN transistor at high temperatures are not developed fully. Moreover, for accurate small signal models, accurate extraction of parasitic resistances, capacitances, and inductances is required, which affects the whole RF characteristics of the devices. To element the effect of the parasitic components from the DUT, several methods have been discussed in the literature, such as open-short, two-step, and three-step de-embedding techniques [29, 30, 31, 32]. However, all the parasitic components are not extracted efficiently using these methods. The most convenient method for extracting parasitic components is known as the cold-FET de-embedding technique [33, 34], where all the parasitic components can be extracted from the cold-FET in various biases. In contrast, the resistance extraction method also has some drawbacks in the research field, because bias dependency of the resistances is overlooked. Although resistances are frequency independent, they are eventually bias dependent. The well-known equation for resistance extraction contains three basic equations constructed

through Z-parameters with four unknown variables [23, 35]. Hence, another equation or relationship is required to determine the values of the unknown parameters. Although there are various straightforward research methods for building an additional relationship, none of them are clearly evaluated. As shown in the Figure.1(c), the equivalent circuit topology that was depicted for the determination of intrinsic elements g_m, g_d, C_{gs}, C_{gd}, C_{ds}, R_i, R_{ds}, and τ. And the extrinsic elements are C_{pg}, C_{pd}, C_{pgd}, R_g, R_s, R_d, $L_{g.pad}$, $L_{d.pad}$, L_s, $L_{g_ex_line}$, and $L_{d_ex_line}$. This also included line inductance in our reference circuit to obtain better accuracy.



(a) A typical RF AlGaN/GaN HEMT device with L_g = 100 nm and $W_g = 2 \times 50$ μm.



(b) Small Signal equivalent circuit of AlGaN/GaN HEMTs device.

Figure 1.5: (a) Typical GaN HEMT (RF device) and (b) Small Signal equivalent circuit of GaN HEMT.

At high frequencies, the effect of parasitic capacitances is negligible, while the effects of resistances and inductances are introduced and considered. Under a cold bias condition ($V_{ds} = 0$), the basic equation for resistance extraction can be written as follows:

$$R_S + R_g + \frac{R_{ch}}{3} = \mathrm{Re}(Z_{11}) \tag{1.6}$$

$$R_S + \frac{R_{ch}}{2} = \mathrm{Re}(Z_{12}) \tag{1.7}$$

$$R_d + R_g + R_{ch} = \mathrm{Re}(Z_{22}) \tag{1.8}$$

These three equations are constructed with four unknown variables. Most of the existing research methodology uses approximations to determine the fourth unknown variable or the high-frequency channel resistance value is ignored. Lu et al. [36] obtained the value of R_s+R_d under a cold-pinched off (V_{gs} < V_{th}, V_{ds} =$0V$) condition. However, there was no maximum or minimum limit included for the V_{gs} pinch-off condition and the process of extraction were not stated clearly. Dambrine et al. [23] postulated four conditions about the extraction of another unknown variable, which included the conventional method [37]. In their method, the series resistance (R_s) calculation in the DC method always provided higher values, which would be questionable and possibly problematic when calculating the channel resistance from Equation (2). There was also a difference between the DC method and the RF method for resistance extraction. Therefore, fluctuation of the resistance values is inevitable, resulting in incorrect results.

To overcome these difficulties and the unstable behavior of resistances, we proposed a new method for building the relationship between drain and source resistances that can be expressed with one additional equation. At the cold-FET condition (V_{ds} =0 V), the drain current (I_d) is not theoretically flowing, although a small fraction of I_d can flow practically, which is visible from the measured RF data. In this case, the drain current does not discernably change the potential distribution inside the channel and the superposition principle is applied to obtain the drain-source voltage [38], as follows:

$$V_{ds} = (R_s + R_d + R_{ch})I_d + \left(R_s + \frac{R_{ch}}{2}\right)I_g \tag{1.9}$$

$$\frac{-I_g}{I_d} = \frac{(R_s + R_d + R_{ch})}{R_s + \frac{R_{ch}}{2}} \tag{1.10}$$

The results and discussion mentioned elsewhere [39]. After determining the ratio of I_g/I_d, there can be obtained a relationship between source and drain resistance. In addition, there are two parameters that need to be considered for the frequency determination: 1) the current gain

cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}). For simplicity, here we mentioned the equation of the cut-off frequency which can be expressed by [40],

$$f_T = \frac{g_m}{2\pi}\left[\left(c_{gs} + c_{gd}\right)\left(1 + \frac{R_d + R_s}{R_{ds}}\right) + c_{gd}\, g_m (R_d + R_s)\right]^{-1} \tag{1.11}$$

And the maximum oscillation frequency is given by [40]:

$$f_{\max} = \frac{f_T}{\sqrt{4\frac{R_s + R_g + R_{gs}}{R_{ds}} + 2\frac{c_{gd}}{c_{gs}}\left(\frac{c_{gd}}{c_{gs}} + g_m\left(R_s + R_{gs}\right)\right)}} \tag{1.12}$$

1.4 Motivation

The motivation for this thesis arises from the significant challenges faced in the widespread adoption of GaN HEMT technology, particularly concerning its electrical reliability. While GaN HEMTs exhibit robustness against various electrical overstress conditions, ensuring long-term reliability becomes a critical concern. Mean Time To Failure (MTTF) is a pivotal parameter in assessing device longevity, typically extrapolated from high-temperature stress tests to standard operational temperatures. Long-term reliability tests, conducted over extended periods and under different temperature conditions, are commonly used to determine device reliability. However, despite these tests, the precise estimation of MTTF has remained elusive in many cases.

The study aims to address this gap by comprehensively exploring the effects of electrical field stress on long-term reliability, with a particular focus on the GaN HEMTs. It delves into the underlying physical mechanisms responsible for device degradation, which include hot electron-induced trap effects and impact ionization. The precise determination of MTTF values, influenced not only by temperature but also by the electric field stress conditions, is of paramount importance. The goal is to gain a deeper understanding of the degradation mechanisms and their impacts, allowing for the deliberate design of device structures to optimize both performance and reliability.

To ensure robust reliability, it is imperative to cultivate an intricate comprehension of the underlying physical mechanisms governing device degradation. This necessitates a comprehensive exploration of the stress conditions, encompassing current, voltage, temperature,

and environmental factors that precipitate degradation. Furthermore, given the typical trade-off between performance and reliability, a thorough comprehension of the physics of degradation empowers the deliberate design of the device structure and heterostructure to achieve a harmonized optimization of both performance and reliability. In this thesis, we mainly focused degradation of the drain current (I_{ds}), threshold voltage shift (ΔV_T), transconductance (G_{max}), on-resistance (R_{on}) and gate leakage current (I_{g_leak}) at different bias condition of HTOL test.

The method of MTTF (mean-time-to-failure) values were determined by combined accerleration factor (voltage and temperature). Device reliability is typically assessed in terms of lifetime, which is determined through stress tests involving elevated temperatures and/or more stringent bias conditions to accelerate degradation. A sound understanding of the physical degradation mechanisms enables the accurate determination of acceleration parameters like temperature and voltage for these stress tests, leading to precise predictions of device lifetime. This study carried out systematic and comprehensive analysis of reliability and failure mechanism in AlGaN/GaN HEMTs depending on buffer, barrier and channel design.

1.5 Background

In this section, we present an overview of prior research endeavors documented in the literature concerning the reliability of GaN technology. To begin, we provide a concise compilation of the most noteworthy findings from studies addressing degradation in GaN High Electron Mobility Transistors (HEMTs). In the subsequent sections, we delve into a more comprehensive exploration of what seem to be the two predominant degradation mechanisms: firstly, the hot electron effects, and secondly, the formation of defects induced by the inverse piezoelectric effect. To conclude this section, we also scrutinize two associated phenomena, namely trapping effects, and current collapse.

1.5.1 Reliability Studies

The electrical deterioration of GaN High Electron Mobility Transistors (HEMTs) has been subject to extensive investigation by numerous researchers. As previously noted, the decrease in drain current and output power stands as a prominent and vexing issue in the realm of RF power applications, a phenomenon that has been extensively documented across diverse

stress experiments [41]. GaN microwave HEMTs face reliability issues due to the properties of the materials used and the quality of their growth process. Figure 1.6 presents a schematic cross-section of an AlGaN/GaN HEMT and provides an overview of the primary failure mechanisms documented in the literature, which will be briefly summarized below:

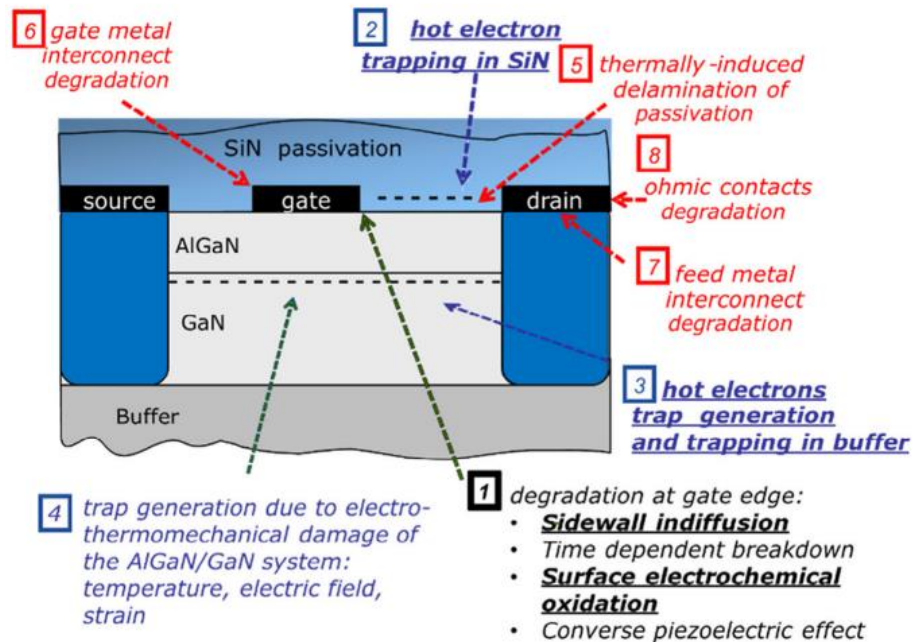


Figure 1.6: A schematic cross-section of an AlGaN/GaN high electron mobility transistor (HEMT) illustrates prevalent failure mechanisms described in the literature. Reprinted from [41] with permission of *IEEE*.

1.5.2 Inverse Piezoelectric Effect :

The hypothesis of inverse piezoelectric effect was first proposed by Joh et.al in terms of the GaN HEMTs degradation mechanism [17]. The semiconductor layers on the drain side of the gate edge in a GaN HEMT represent the most crucial region, where the highest levels of current density, electric field, and local temperature converge simultaneously. In this position, several degradation mechanisms are expedited: owing to GaN's piezoelectric properties, the application of an electric field intensifies tensile stress within the AlGaN barrier. This stress relaxation, in

turn, leads to the formation of lattice defects or even cracks, ultimately resulting in the deterioration of drain current (I_D) and increase in gate leakage current (I_G).

This phenomenon is depicted in Figure 1.7. Because of the inherent lattice mismatch between AlGaN and GaN, the AlGaN barrier layer is inherently under tensile strain, even in the absence of an electric field, resulting in the accumulation of elastic energy. When an electric field is applied, the tensile stress induced by the inverse piezoelectric effect compounds with this pre-existing strain due to lattice mismatch.

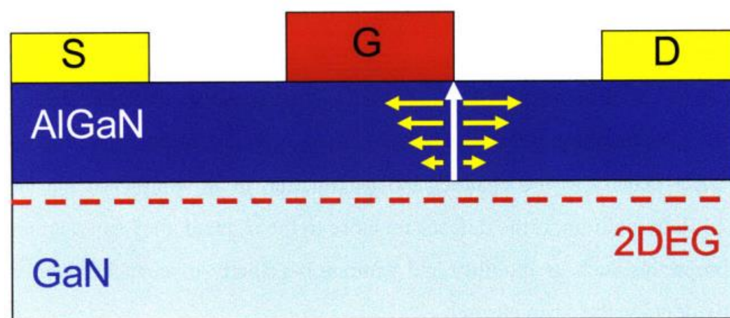


Figure 1.7 : Inverse piezoelectric effect at the gate edge in the drain side of GaN HEMT. The vertical and horizontal arrows represent vertical electric field and mechanical stress, respectively. Reprinted from [42] with permission of Elsevier.

Consequently, the elastic energy density within the AlGaN layer increases. If this cumulative elastic energy density surpasses a critical threshold, it can lead to the formation of crystallographic defects, such as dislocations or cracks. Many research groups investigated inverse piezoelectric effect [43-45]. Although inverse piezo-electric effect is the dominant mechanism in off-state stress condition, it is not only one degradation mechanism in GaN HEMTs.

1.5.3 Electrochemical GaN Oxidation: Gate Metal Interdiffusion

Under the influence of elevated temperatures and strong electric fields, gate metals and contaminants have the propensity to migrate towards the semiconductor surface, particularly at the sidewall interface between the metal and passivation layer (typically Si_xN_y). This phenomenon has been documented to involve the interdiffusion of elements such as Au and O,

among others [46]. Under specific conditions, which include the presence of moisture, elevated temperatures, high electric fields, and device current, oxygen has the potential to undergo a reactive process with GaN at the device surface. This reaction can result in the formation of pits and voids near the gate edges, leading to an increase in parasitic resistance within the access regions and a subsequent reduction in transconductance. The electrochemical dissolution of GaN has the capacity to initiate a gradual structural deterioration along the drain edge of the gate. This deterioration is characterized by the emergence of pits and grooves and is closely linked to the presence of oxygen or water vapor, resulting in the creation of Ga and Al oxide compounds. In extreme instances, this phenomenon has been observed to culminate in the nearly complete replacement of nickel (Ni) by gold (Au) [47]. Figure 1.8 illustrates the transmission electron microscopy (TEM) cross-sections of gate modules both before and after undergoing stress.

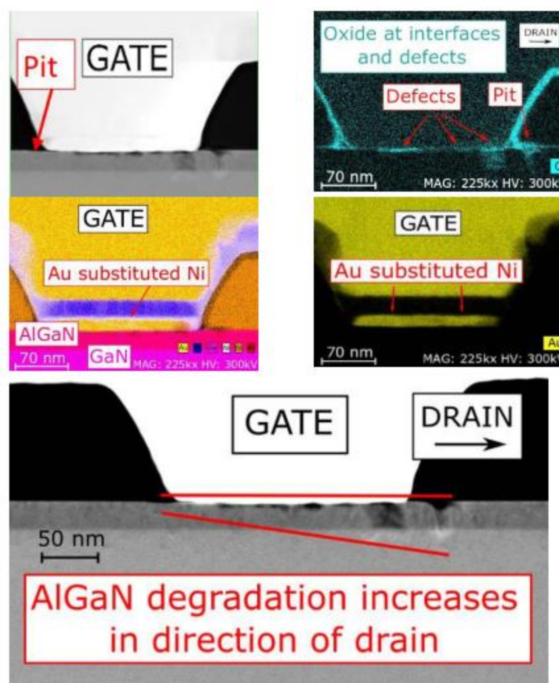


Figure 1.8: (Left) EDX map of oxygen within the TEM cross section of a 0.25-µm gate AlGaN/GaN HEMT after 24 h at V_{DS} = 30 V, V_{GS} = 0 V, and P_D = 22 W/mm. (Right) EDX map of Al (red), Si (dark orange), Ni (white), Ga (purple), Pt (blue), and Au (yellow), showing slight Au diffusion at the gate borders, but uniform Ni Schottky contact. O is found in correspondence of a pit on the gate–drain AlGaN surface. Drain contact toward right in the figure. Reprinted from [51] with permission of IEEE.

Commonly reported indicators of degradation related to gate-metal diffusions involve alterations in Schottky characteristics over time. These changes encompass an escalation in gate-leakage current [48, 49] and a shift in the threshold voltage. It's worth mentioning that the V_T -

shift is attributed to changes in the Schottky barrier height Φ_{SBH} [51, 52]. Collectively, these effects can result in a reduction in carrier concentration within the 2D electron gas (2DEG) and a decrease in saturation current (I_{DSS}).

1.5.4 Hot Electron Effect:

The hot electron effect in Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) is a phenomenon that occurs when high-energy electrons gain excess kinetic energy in the device, leading to various performance and reliability issues. In GaN HEMTs, electrons are the charge carriers responsible for carrying electrical current. When a high electric field is applied to the device, either during normal operation or under stress conditions, some electrons can acquire significant amounts of energy. As these high-energy electrons move through the device, they can collide with lattice atoms and scatter. During these collisions, some of their excess energy is transferred to the lattice, leading to lattice heating. The "hot electrons" do not stay confined within the channel, as depicted in Figure 1.9. Instead, they can be captured in various locations: 1) Some of these high-energy electrons may get trapped within the AlGaN layer situated beneath the gate, 2) Others can become trapped in the gate-drain region, which experiences the highest electric field intensity, these electrons may be located at the surface or within the silicon nitride passivation layer and 3) Additionally, some hot electrons might be captured within buffer traps.

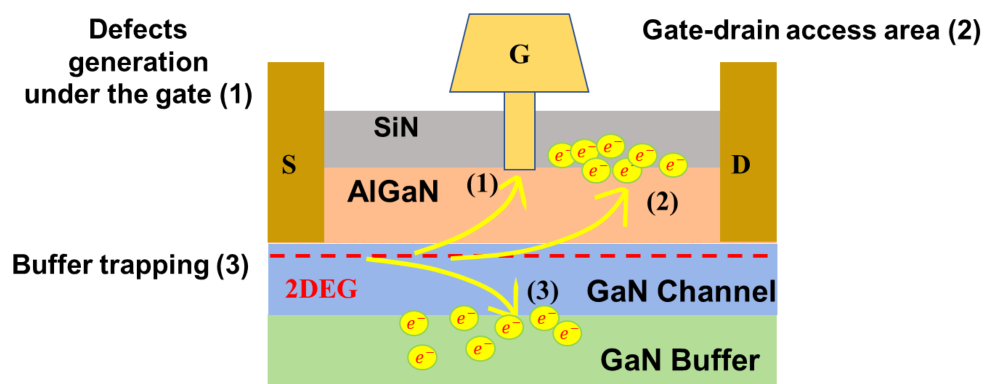


Figure 1.9 : Schematic HEMT cross-section showing possible mechanisms of hot-electron-induced degradation :defects generation under the gate (1); in the gate-drain access area and electron trapping in the SiN passivation (2); buffer trapping (3).

A more comprehensive characterization can be attained through the measurement of electroluminescence (EL) generated by hot electrons (HE). The precise mechanism responsible for EL has been a subject of ongoing debate. Hot-electron characterization was conducted through electroluminescence (EL) microscopy, utilizing a charge-coupled device (CCD) camera with a spectral response ranging from 300 to 1100 nm, reaching up to 95% efficiency at 600 nm. This setup was coupled with an optical microscope. EL, resulting from intraband transitions of high-energy electrons or band-to-band electron-hole recombination processes, serves as an alternative means to assess the effects of hot electrons, instead of relying on gate current measurements [53]. Figure 1.10 shows the nonmonotonic behavior of EL intensity as a function of gate bias V_{GS} [54]. As the gate-source voltage (V_{GS}) surpasses the pinch-off threshold, carriers begin to flow within the channel, and they experience a heating effect caused by the high electric field in the gate-drain region. Consequently, light emission is detected, and its intensity escalates with increasing V_{GS}, owing to a larger population of primary electrons in the channel (refer to Figure 1.9). Simultaneously, however, the gate-drain voltage, and thus the electric field, diminishes as V_{GS} rises. Beyond a certain V_{GS} threshold, electrons become less energetic, leading to a decline in emitted light. By measuring electroluminescence (EL) intensity as a function of both V_{DS} and V_{GS}, one can assess the degree of "hot-electron-stress" imposed on the device under examination. Additionally, EL micrographs provide insights into current density uniformity and the presence of gate leakage paths.

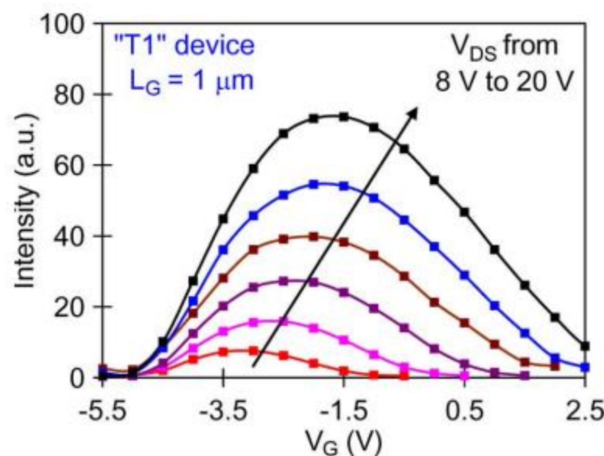


Figure 1.10 : EL intensity in a "T1" device as a function of VGS from pinch-off (∼−5.5 to +2.5 V) at various VDS from 8 to 20 V, step 2.4 V. A nonmonotonic behavior typical of phenomena induced by hot carrier is observed.

Under pinch-off conditions, the quantity of hot electrons is at its minimum, although the few hot electrons present possess greater energy due to the amplified electric fields [55, 56]. In the off-state, electroluminescence (EL) has been correlated with gate leakage, signifying the presence of electrons being introduced from the gate [57]. Moreover, it has been observed that hot electrons tend to inflict less damage during RF (radio frequency) stress tests compared to DC (direct current) stress tests [58].

1.5.5 Trapping Effect:

There have been reports indicating that GaN HEMTs are susceptible to significant trapping effects [9]. Historically, the understanding of current-related trapping effects originated from the work of Khan et al [59]. An observable reduction in current was noted in the AlGaN/GaN High Electron Mobility Transistor (HEMT), both before and after subjecting it to a high drain bias. This phenomenon is commonly referred to as "current collapse," "slump," or "dispersion." The current reduction is caused by electron trapping. There are lots of research related to trapping phenomena which includes donor-like trap, acceptor-like trap, surface trap, trap in the channel, deep level trapping in buffer layer [60, 61].

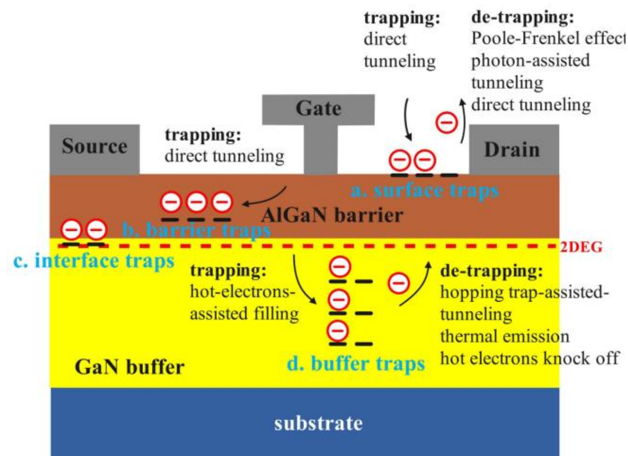


Figure 1.11 : Main trapping behaviors in the AlGaN/GaN HEMT. Trapping condition for (a) surface traps: high negative gate voltage (V_G); (b) barrier traps and (c) interface traps : negative V_G or V_G > threshold voltage & drain voltage (V_D) > 0 V; d) buffer traps : high V_D. Reprinted with the permission of reference [61].

Primarily, the phenomena observed in AlGaN/GaN HEMTs, as mentioned above, are fundamentally attributed to the trapping and detrapping processes of electrons in unintended locations. As illustrated in Figure 1.11, when a high negative gate voltage is applied, electrons become trapped at the device surface due to direct tunneling. During on-state operation, where the gate voltage exceeds the threshold voltage and the drain voltage is greater than 0V, electrons can tunnel into the barrier or interface, leading to trapping effects. If the drain voltage is sufficiently high, the hot electrons may become trapped within the buffer layer [62]. Although the gate-lag arises from traps within the surface, buffer, and interface regions, it is primarily influenced by the surface traps based on the measurement configuration. The application of different gate voltages induces electrons to undergo trapping and detrapping processes at the surface.

The drain-lag phenomenon is attributed to traps within the buffer, barrier, and interface regions. When the drain voltage is applied, it propels electrons in the channel near the gate region into the barrier and buffer layers, where they are more susceptible to being captured by deep-level traps. Consequently, trapping and detrapping within the buffer are more influential in the context of drain-lag measurements [62].

Trapping effects also attributed by Hot electrons present in the channel. The term "hot electrons" denotes nonequilibrium electrons that gain enough kinetic energy to surpass potential energy barriers. These electrons can then be injected into buffer, barrier, or insulating layers and become trapped. They have the ability to break atomic bonds, generate interface states, or activate traps. One such example is the process of dehydrogenation [9]. In AlGaAs/GaAs High Electron Mobility Transistors (HEMTs), the impact ionization hole current gives rise to a negative gate current (Ig), which can be associated with the hot-electron effect [63].

In summary, various measurement techniques elicit distinct trapping behaviors and phenomena. Transient current measurements and pulsed I_{DS}-V_{DS} measurements are the most commonly employed methods to investigate trapping effects. Other measurement approaches are utilized in specific scenarios, such as DC conditions or power amplifier applications.

1.6 Structure of this work

This thesis represents an expansion of our earlier research [64-67]. Within this thesis, we conduct a systematic investigation aimed at comprehending the intricate physical mechanisms

responsible for the electrical degradation observed in GaN High Electron Mobility Transistors (HEMTs). Our previous research primarily emphasized reliability experiments under simplified stress conditions, seeking to establish a broad overview of device degradation mechanisms, in this thesis, we delve into a more comprehensive examination of the electrical degradation of GaN High Electron Mobility Transistors (HEMTs, exploring the details in greater depth. This includes both short and long-term reliability assessment according to various stress conditions (off-state step stress, V_{DS} = 0 V step stress and On-state stress). Detailed analysis of channel temperature prediction in 3-temperature DC lifetime test which plays a significant role in MTTF prediction of the devices.

The methodology of determining MTTF with combined acceleration factors (both voltage and temperature related) is also presented. The physics of electrical degradation which is related to the hot electron effect and hot electron induced impact ionization is the primary focus in this thesis. Employing a systematic approach, we aim to uncover a more comprehensive understanding of the fundamental mechanisms that underlie device failure.

The thesis is organized as follows: In Chapter 2, the methodology related to reliability assessment is briefly described. An overview of mathematical concepts such as Mean-time-to-failure (MTTF), the Arrhenius model, and the Eyring model is introduced. The discussion also covers the test wafers and the test methods, including the experimental setup and characterization methodology.

In Chapter 3, the main experimental outcomes are demonstrated. The impact of various stress conditions on the devices is presented, including gate current degradation mechanisms and threshold voltage instability. In the HTOL (high temperature operating lifetime) test, the importance of predicting channel temperature for long-term reliability is discussed. A simple empirical model of channel temperature is presented and compared with experimental results as well as TCAD Silvaco simulations. Finally, MTTF determination through combined acceleration factors is shown.

In Chapter 4, we delve into the effects of electrical field stress on long-term reliability. The experiments provide clear evidence that MTTF values are influenced not only by temperature but also significantly by the electric field stress conditions.

Chapter 5 discusses the physics of electrical degradation of the devices after stress. The main mechanism of electrical degradation is evaluated through a comparison of different HEMT structures (three different HEMT structures). The focus of the degradation is on the hot electron effect and hot electron-induced impact ionization.

Ultimately, the research findings are summarized in Chapter 6. Drawing from our conclusions, we offer device design guidelines to enhance reliability. This chapter also provides suggestions for future research endeavors.

Chapter 2

Reliability Methodology

This chapter starts with an introduction of mathematical overview of reliability. The reliability model such as Arrhenius, Eyring, inverse power law is briefly discussed which are essential to predict mean-time-to-failure (MTTF). Finally, the method of determining MTTF by combined acceleration factor focusing on voltage and temperature as stressors are presented.

2.1 A Mathematical Perspective of Mean-time-to-failure (MTTF)

The IEEE (Institute of Electrical and Electronics Engineers) defines reliability as the capacity of an item to fulfill a specified function under prescribed conditions for a predetermined duration [68]. Conventional reliability calculations rely on statistical data derived from the collection of failure records. For a set of n statistically identical and independent items, data on the duration between the initiation of device usage and the onset of failure can be gathered. This information can then be employed to calculate the empirical expected value for the average failure-free time, τ as

$$E^{\wedge}[\tau] = \frac{t_1 + t_2 + t_3 + \ldots\ldots + t_n}{n} \tag{2.1}$$

For $n \to \infty, E^{\wedge}[\tau]$ This converges to the expectation value, denoted as E[τ], which represents the mean time-to-failure (MTTF). The time-dependent failure density, denoted as *f(t),* is characterized using probability density functions. The number of devices that fail until a certain time is described using the cumulative distribution function *F(t)*,

$$F(t) = \int_0^t f(t^{'})dt^{'} \tag{2.2}$$

The proportion of items that have not experienced failure up to time t can be expressed through the use of the survival or reliability function,

$$R(t) = 1 - F(t) \tag{2.3}$$

Frequently, the hazard rate, denoted as λ, is employed to describe the failure behavior of items. It defines, at a specific time, the ratio between items that have failed and those that are still operational. It is formulated as follows:

$$\lambda = -\frac{dR(t)}{dt}\frac{1}{R(t)} = \frac{f(t)}{1 - F(t)} \tag{2.4}$$

With a specified failure rate, the reliability function can be deduced from the following:

$$R(t) = e^{\left(-\int_0^t \lambda(t')dt'\right)} \tag{2.5}$$

And in semiconductor devices, as a rule, lack repair and maintenance options once a component experiences failure. Consequently, they fall under the category of non-repairable or non-maintainable products. The average time for non-repairable components, encompassing devices, parts, and elements, to reach failure is defined as the Mean Time to Failure (MTTF) and can be expressed through the following equation: the *Mean Time To Failure* (MTTF) can be derived as

$$MTTF = \int_0^\infty tf(t)dt \tag{2.6}$$

Various failure distributions, denoted as *f(t),* have been employed to characterize failure events in devices and systems. A convenient modeling approach involves the utilization of a constant failure rate. A particular case of significance in reliability engineering arises when the hazard rate can be regarded as constant (λ=constant). This represents the typical rate of failure during the standard lifecycle of long-life devices, excluding the initial infant mortality and the ultimate wear-out stages. In this case, the equations (2.3) and (2.4) can be written as

$$R(t) = e^{(-\lambda t)} = 1 - F(t) \tag{2.7}$$

$$f(t) = \lambda e^{(-\lambda t)} \tag{2.8}$$

Using λ = cost, using (2.8) in (2.6) gives the relationship between λ and MTTF is MTTF = 1/λ. MTTF is become reciprocal of failure rate.

2.2 Arrhenius Model

The degradation and deterioration of materials primarily stem from alterations at the atomic and molecular levels. These mechanisms encompass processes such as diffusion, oxidation, adsorption, dislocation or displacement, electrolysis, and the formation of corrosion cracks. The cumulative progression of these changes gradually deteriorates the material and components, eventually surpassing a specific threshold and culminating in failure. This conceptual framework is commonly referred to as the reaction theory model. Notably, within the transition from normal conditions to deteriorated conditions, there exists a critical energy threshold. In order to surpass this threshold, the requisite energy must be sourced from the surrounding environment. This critical energy level is referred to as the activation energy. The relationship between reaction rates and temperature was first elucidated by Arrhenius, and his discovery gave rise to the widely employed Arrhenius equation [69]. The Arrhenius equation is a fundamental determinant of the rate at which numerous chemical processes occur. A reaction rate can be defined for a wide range of both physical and chemical processes as below:

$$R = A\exp\left(-\frac{E_a}{kT}\right) \tag{2.9}$$

Where,

A = Reaction rate constant

E_a = Activation Energy (eV)

k = Boltzmann Constant [8.617×10^{-5} (eV/ K)]

T = Absolute temperature (K)

If the time-to-failure is t_f , then

$$t_f = A\exp(\frac{E_a}{kT}) \tag{2.10}$$

And by taking the logarithm of both sides of the equation that gives

$$\ln t_f = \ln A + \frac{E_a}{kT} \tag{2.11}$$

This equation represents the logarithmic lifetime (t_f) plotted against the reciprocal of the temperature following the linear equation of straight line, and the slope if the straight line demonstrated the activation energy (E_a). Subsequently, based on this concept, the acceleration

coefficient between two specified temperatures can be calculated. For instance, if t_{f1} and t_{f2} represents the lifetimes at T_1 and T_2 respectively, then

$$\ln\left(\frac{t_{f1}}{t_{f2}}\right) = \frac{1}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)E_a \tag{2.12}$$

This equation yields an acceleration factor that can be used to ascertain the activation energy of a reaction. Figure 2.1 illustrates a schematic representation of this concept.

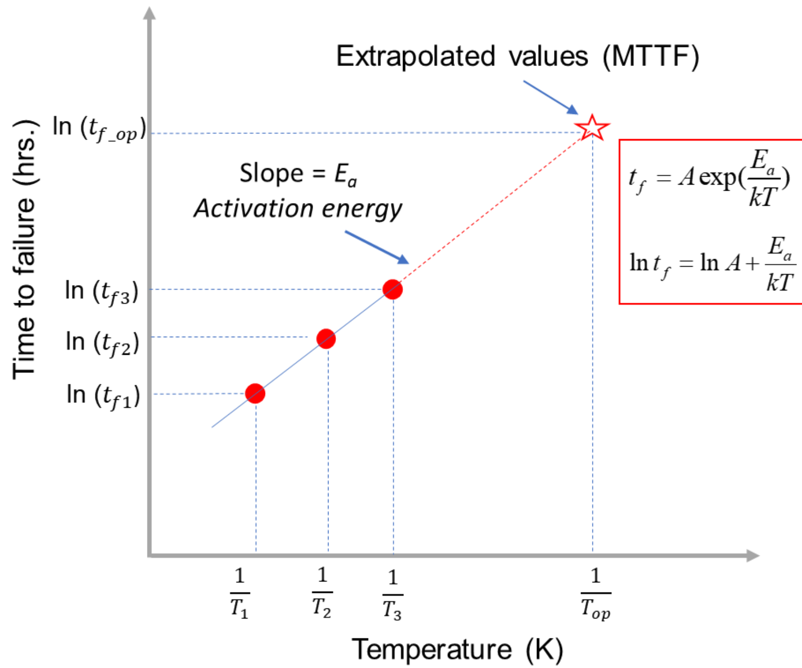


Figure 2.1 : Schematic of the Arrhenius Model

Plotting the normal cumulative percent-failure against the logarithm of time (as described in equation 2.12) allows for the determination of the median lifetime at a specific temperature**.** In general, a life test should be conducted at a minimum of three distinct temperatures to yield a reliable estimate for the activation energy. Another valuable parameter is the ***Acceleration Factor***, defined as the ratio between the median lifetime at two different temperatures. This can be expressed as below equation:

$$A_f = \frac{t_{f1}}{t_{f2}} = \exp\left\{\frac{E_a}{k}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]\right\} \tag{2.13}$$

Therefore, at a temperature T_{stress}, time to failure is given by $t_{fstress}$ and the estimated time to failure t_f at temperature T can be expressed as [70, 71]

$$t_f = A_f . t_{fstress} \tag{2.14}$$

2.3 Eyring Model

While the Arrhenius model highlights the influence of temperature on reactions, the Eyring model is frequently employed to illustrate the impact of various stress factors beyond temperature, including mechanical stress, humidity, and voltage. The standard equation of the Eying model is as follows [72],

$$R = A\exp(-\frac{E_a}{kT}).S^{\alpha} \tag{2.15}$$

Where, α = Constants, S is the stress factors other than temperatures and the other parameters are same as Arrhenius equation. When multiple failure mechanisms are present, the Arrhenius relationship can be modified to Eyring's lifetime prediction model. The standard expression for the Eyring model is given as follows:

$$AF(T) = \frac{tf_1}{tf_2} = \left(\frac{V_A}{V_N}\right)^n \exp\frac{E}{k}\left[\frac{1}{T_1} - \frac{1}{T_2}\right] \tag{2.16}$$

Where, V_A = voltage in accelerated condition, V_N = voltage in normal condition, n = voltage acceleration constant. One more term (i.e., stress) can be deleted or added to the conventional Eyring model, depending on different Physics of failure (PoF) mechanisms. The total activation energy corresponds to the minimal energy required to activate the weakest failure mechanism when many failure mechanisms are present.

2.4 Combined Acceleration factor

Voltage and temperature are two pivotal stress factors in the analysis of semiconductor device reliability, particularly in accelerated testing. To date, a significant portion of research efforts has been concentrated on investigating the acceleration effects of voltage and temperature on individual failure mechanisms. Before diving into the deep, we need to be clear about the importance of combined acceleration factor. In general case, MTTF is determined by Arrhenius model which emphasizes only one stress parameter called temperature, but AlGaN/GaN HEMTs

deals with multiple degradation mechanisms that results in different MTTF values at different bias zone or condition (10^7 hrs. at hot electron zone, 10^5 – 10^6 at electron trapping zone and 10^5 at surface pitting zone) [58]. The 3-temperature DC test only focuses on the effect of temperature at one specific voltage stress, while the combined effect of both temperature and voltage needs to be considered in terms of the long-term reliability of the devices [73, 74].

Figure 2.2 represents three values of MTTF ($MTTF_1$, $MTTF_2$, $MTTF_3$) corresponding to three distinct voltage stress conditions. Additionally, the channel temperatures (T_{ch}) differ for each stress condition. The activation energy (E_a) varies for each failure mechanism. This figure conclusively demonstrates that the failure mechanism is not uniform and depends on the bias condition or zone. Consequently, it is not feasible to define the failure analysis perfectly solely based on the extracted values of E_a. Furthermore, alongside the activation energy (E_a), it is imperative to consider the voltage-dependent acceleration factor.

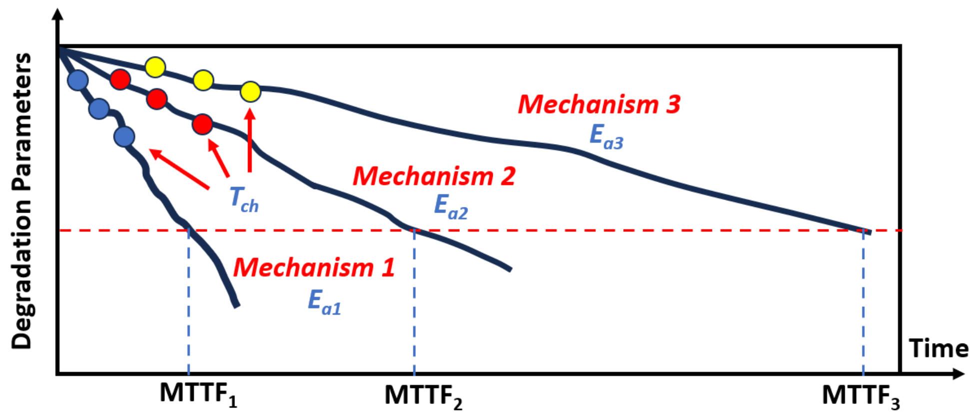


Figure 2.2 : Multiple degradation mechanisms of AlGaN/GaN HEMTs.

In Figure 2.2, various degradation mechanisms (depending on the bias zone) exhibit distinct activation energies (E_{a1} , E_{a2}, and E_{a3}) [58]. The bias zones do not have precise boundaries and may vary from one device to another. Moreover, the hypothesis does not consider high voltage or high power zones in the stress conditions.

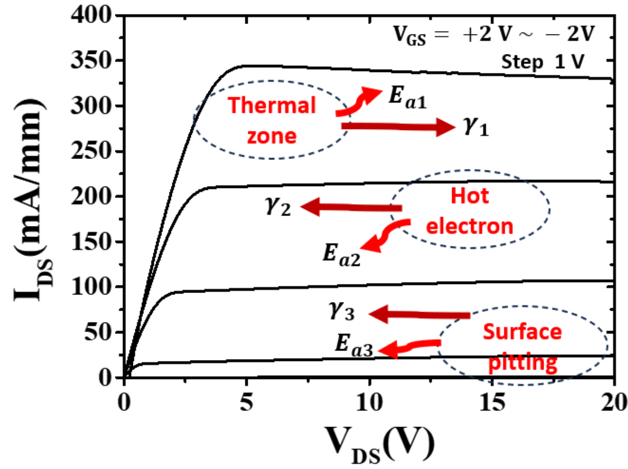


Figure 2.3: Typical output characteristics of AlGaN/GaN HEMT and possible degradation mechanism depending on the bias zone. Along with activation energy (E_a), voltage acceleration factor (γ) is added for each zone.

To elucidate the impact of voltage/electric field in the long-term reliability test, we have proposed a novel acceleration factor called voltage acceleration (γ), which comprehensively calculates the MTTF values. The modified acceleration factor equation can be expressed as follows:

$$AF = e^{\left\{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right\}} \times e^{\{\gamma(V_{stress} - V_{use})\}} \tag{2.17}$$

where, k = Boltzmann constant, T_{use} = temperature at normal operating condition, T_{stress} = temperature at stressed condition, V_{use} = voltage at normal operating condition and V_{stress} = voltage at stressed condition. The popularity of this multiplication model has grown due to its simplicity in applying reliability projections, eliminating the need to construct a complex lifetime model that accommodates a range of temperatures and voltages. In this work, the combined effect of voltage and temperature will be discussed from the reliability perspective of on-wafer devices.

2.5 Reliability test wafers

Figure 2.4 shows a schematic cross section of a AlGaN/GaN HEMTs for this experiment. Only the Epi wafers are fabricated by our industrial collaborators, Korea advanced nano fab center (KANC), Republic of Korea and Nippon Telegraph and Telephone (NTT), Japan. The

AlGaN/GaN HEMTs is grown by metal-organic chemica vapor depositon (MOCVD) on Sapphire and semi-insulating SiC. After that rest of the fabrication and processes are completed by our side. AlGaN/GaN HEMTs we have studied in this experiment typically source-to-drain distance (L_{SD}) is between 2 µm to 8 µm, a gate length (L_G) from 3 µm to 14 µm, gate width (W_G) is 50 µm.

Nonetheless, the fabrication of nitride semiconductor devices poses a relatively complex challenge owing to their exceptional stability. For instance, the etching of nitride materials is a particularly intricate process. The absence of a consistent wet etching method necessitates the use of dry etching techniques, such as chlorine-based plasma reactive ion etching. However, dry etching methods often risk compromising the electrical properties of nitride semiconductors and can lead to surface damage. Establishing reliable ohmic contacts on nitride semiconductors can also be challenging. The choice of metals (e.g., Ti, Al, Ni, Au, Mo), their stacking configuration, and thickness all significantly influence the Ohmic contact resistance.

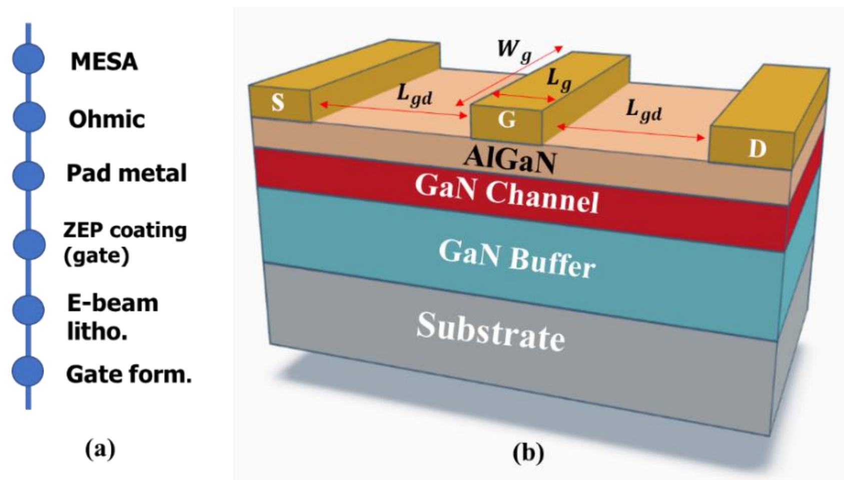


Figure 2.4 : (a) Process flow of metal contact formation and (b) Schematic cross-section of AlGaN/GaN HEMTs.

A mesa structure is formed, typically with a step height ranging from 100 to 180 nm. To achieve selective etching of AlGaN and GaN in specific areas, a photoresist is employed as an etch mask. Ensuring reliable dry etching and mesa-isolation requires fine-tuning various processing parameters, including ICP/RF powers, chamber pressure, and temperature. The effects of dry etching concerning these processing parameters are detailed in Figure 2.5 (c).

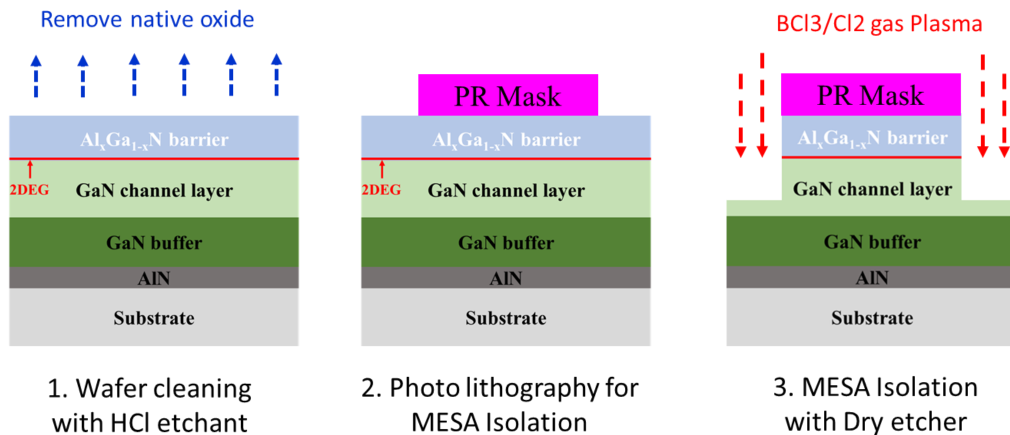


Figure 2.5 Process flow of Mesa-Isolation technique

The next step is to establish ohmic contacts and the process flow of establishing ohmic contacts are illustrated in Figure 2.6. The contact metallization system involving Ti/Al, along with the use of rapid thermal annealing (RTA), has been the subject of extensive research and is among the most widely investigated systems mentioned in the literature. This work employs Ti/Al/Ni/Au ohmic contacts, with the metal sequence starting from the bottom, which have undergone annealing through rapid thermal annealing (RTA).

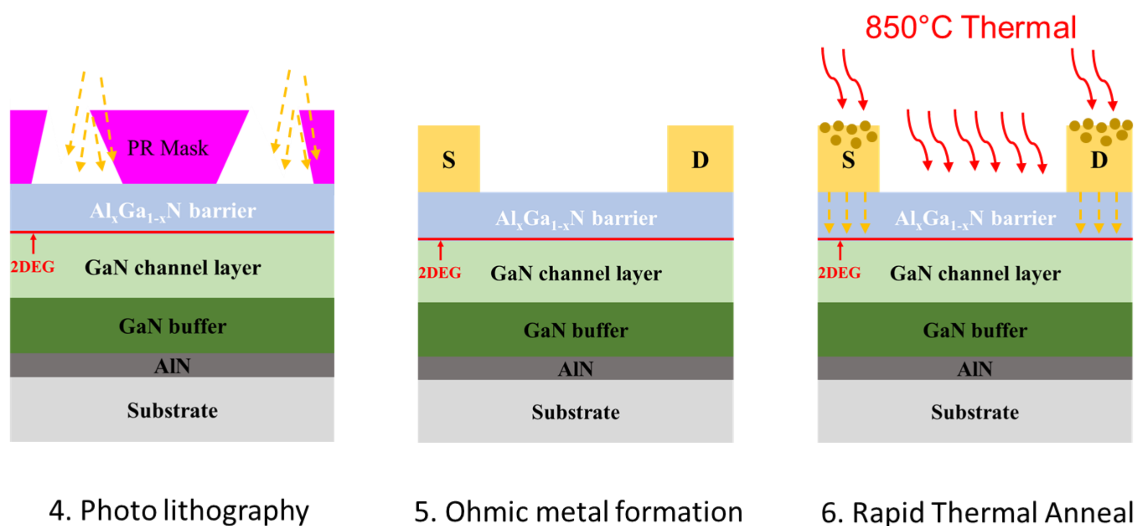


Figure 2.6 : Process flow of Ohmic contact formation.

The gate deposition process is arguably the most intricate and challenging stage in the entire device fabrication. To achieve a reduction in both gate length and gate resistance, gates are typically fabricated with a T-shaped cross-section. After establishing ohmic contacts, a Raith 300pa 100 keV e-beam lithography equipment is employed to fabricate deep-submicron T-gates, with gate lengths measuring less than 100 nm, positioned between the source and drain ohmic contacts. A 100 nm-long T-gate was successfully manufactured and shown in Figure 2.7 which illustrates the two-step e-beam exposure technique including ZEP/PMGI/ZEP tri-layer resist.

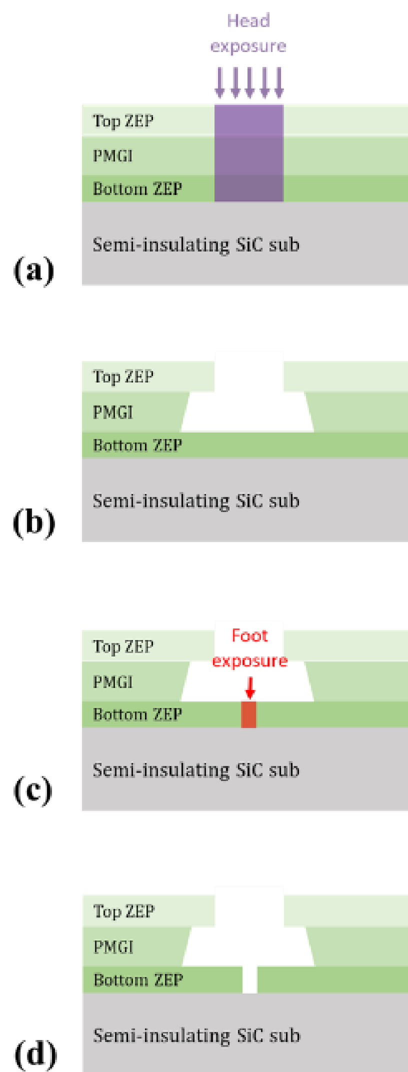


Figure 2.7 : The conventional method for fabricating submicron T-shaped gates involves e-beam lithography. The process includes (a) head exposure, (b) sequential development of top ZEP and middle PMGI for the head, (c) foot exposure, and (d) development of the bottom ZEP for the foot.

2.6 Reliability test experiments

The same approach as previously described in [67] is also employed for analyzing device degradation. Initially, we perform a comprehensive characterization of the device before subjecting it to stress. This characterization encompasses a wide range of I-V characteristics, including output, transfer, gate, and subthreshold measurements. From these measurements, various device parameters are extracted. Subsequently, the device is subjected to a specific stress scheme, with intermittent interruptions to conduct a preliminary device characterization. During these pauses in stress, we extract key figures of merit, including V_T, I_{Dmax}, G_{max}, R_S, R_D, and I_{Goff}. A schematic diagram of the experimental setup is represented in Figure 2.8. It consists of a semiconductor parameter analyzer and a Micro tech probe station. Two different semiconductor parameter analyzer are used: HP4155C and Agilent B1500A (Keysight Technologies, Santa Rosa, CA, USA). The temperature of the base plate of the probe station is regulated using a Temptronic TP03000 ThermoCheck system (inTEST Thermal Solutions GmbH, Deutschland, Germany). For RF characterization, an 8510C Network analyzer was used. The parameter analyzer is managed by a Windows OS PC via a GPIB connection. Certain experiments are conducted in ambient air or under microscope light illumination.

2.7 Type of Stress and methodology

The GaN community commonly employs various stress tests to assess the reliability of the technologies. The following section will provide a brief overview of the most common stress tests, with a particular focus on those utilized in this study.

2.7.1 Off-State Stress

The off-state stress test, often referred to as reverse bias tests, involves biasing the Device Under Test (DUT) under pinch-off conditions. Off-state tests offer the advantage of excluding degradation mechanisms driven by current and provide better control over device temperature. The off-state stress test can be performed using either the step stress method or the constant stress method. In one variation of this test, the drain bias is set to V_{DS} = 0 V, and a negative bias is applied to the gate electrode [75]. The gate electrode is negatively stressed by a certain voltage step of stress for a specific time of duration. In this condition, we can subject both sides of the device to a high electric field simultaneously, but without any channel current. In accelerated aging tests, a high-temperature reverse bias test (HTRB) is conducted, during which the gate

Schottky diode is reverse biased close to the breakdown voltage at high temperatures. This test helps to study the effects of high electric fields and elevated temperatures. In the HTRB condition, the additional drain bias concentration of the electric field occurs at the gate edge on the drain side, resulting in more pronounced degradation in that region.

2.7.2 On-State Stress

The term "on-state stress" typically encompasses all direct current (DC) stress conditions where there is intentionally a non-zero drain current. Therefore, stress tests are also considered to be in the on-state when there is a low quiescent drain current present. One of the most common on-state stress tests is the High-Temperature Operating Life (HTOL) stress test, in which the device under test (DUT) is exposed to a positive drain-source bias, and the gate voltage is set to allow a quiescent current (I_{DQ}) to flow between the source and drain electrodes. HTOL tests can be performed in two ways: either the gate voltage is continuously adjusted to maintain a constant I_{DQ} (referred to as I_{DQ} -stress), or the gate voltage is adjusted initially and then kept fixed for the rest of the test. The constant stress method is used to assess the lifetime distribution under a fixed stress level, keeping the time constant. Assuming the failure mechanism remains consistent, the results obtained from these two methods are expected to align on the same straight line when represented on a graph using either the Arrhenius model or the Eyring model.

The HTOL test is commonly employed to determine the device's lifetime, often referred to as the Mean Time to Failure (MTTF). In this lifetime test, accurately determining the channel temperature is a crucial parameter. Maintaining a constant power throughout the experiment is essential, as any variation can lead to a miscalculation of the lifetime. Figure 2.8 shows the outline of each stress tests methodology.

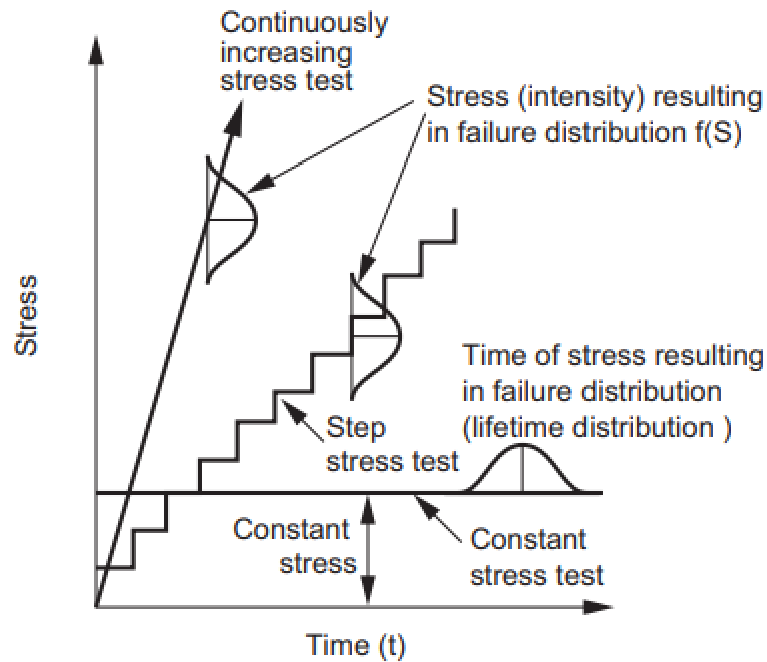


Figure 2.8 : Outline of each stress test methodology. Reprinted from Ref [73]

2.8 Summary

In this chapter, we have introduced GaN HEMTs reliability models, reliability prediction with combined acceleration factors, test wafers and the stress experimental setup in this work. The importance of combined acceleration factors is discussed in greater details. To measure device degradation efficiently, we have developed an automated characterization suite that extracts key figures of merit throughout the stress experiments. In the subsequent chapter, we present the experimental results of our reliability experiments and delve into the phenomena of device degradation.

Chapter 3

Determination of Mean time to failure

In the preceding chapter, we have discussed the experimental setup, characterization methodology, and stress schemes employed to investigate the degradation mechanisms of GaN HEMTs. In this chapter, we present the experimental results of various stress tests. First, we provide a summary of the general results of degradation phenomena from previous work. Building upon the previous findings, we delve into the investigation of degradation in gate current under both off-state stress test and $V_{DS} = 0$ state test. Following this, we explore the long-term reliability aspects, specifically focusing on the HTOL (High-Temperature Operating Life) test. We highlight the significance of precise channel temperature prediction in investigating the Mean-Time-to-Failure (MTTF).

3.1 Summary of previous work

The reliability study initiates with the assessment of the stability of gate metal contacts on AlGaN/GaN HEMTs. The robustness of these contacts is thoroughly investigated via Off-state stress tests, employing both constant and step stress methodologies. [65]. The previous study investigated the comprehensive SBH and temperature as well as device degradation of Ni/Au and Pt/Ti/Pt/Au contacts on AlGaN/GaN HEMTs. The Schottky behavior characteristics for the Ni/Au and Pt/Ti/Pt/Au gate were compared, and the thermal reliability instability was examined at elevated temperatures. In the fabrication process, the Schottky gate contacts were next patterned by photolithography; the Ni/Au (20/300 nm) and Pt/Ti/Pt/Au (8/20/20/300 nm) Schottky gate contacts were fabricated by e-beam evaporation. Figure. 3.1 shows the electrical characteristics (J-V characteristics) of the Ni/Au and Pt/Ti/Pt/Au Schottky contacts on the AlGaN/GaN HEMTs.

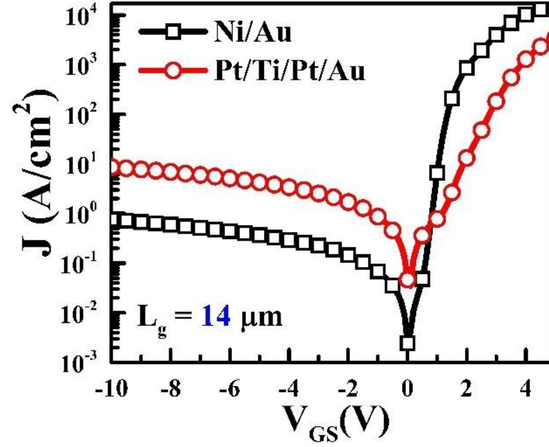


Figure 3.1 : Electrical characteristics of the Schottky contacts made of Ni/Au and Pt/Ti/Pt/Au fabricated on AlGaN/GaN HEMTs at room temperature.

The SBHs and ideality factors for the Ni/Au and Pt/Ti/Pt/Au AlGaN/GaN HEMTs are given by (1) and (2), respectively:

$$J = J_S\left(\frac{qV}{nkT}\right)\left[1-\exp\left(\frac{qV}{nkT}\right)\right] \tag{3.1}$$

$$J_S = A^*T^2\exp\left(\frac{-q\phi_b}{kT}\right) \tag{3.2}$$

Where J_S is the reverse saturation current density, n is the ideality factor, A* is the effective Richardson constant, T is the absolute temperature, ϕ_b is the SBH obtained from the saturation current density, and k is the Boltzmann constant. The SBH of the Pt/Ti/Pt/Au contact at the reverse-biased region was observed to deteriorate, implying that the surface roughness caused by the high-energy Pt atoms deposited during E-beam evaporation process on the AlGaN/GaN HEMTs ultimately caused cracks in the MS contacts. This phenomenon can be attributed to the inhomogeneities at the MS interface and large deviations in the behaviors of the top electrodes despite the higher work function of Pt compared with Ni. Therefore, the reverse leakage current of the Pt/Ti/Pt/Au Schottky contact is higher than that of the Ni/Au contact.

The critical voltage was determined via incrementally stepped stress values of the V_G from -10 V, with the source and drain terminals grounded to avoid self-heating. At each stress step, similar gate length devices from each wafer were stressed for 1 min. To verify the degradation of the SBH under the off-state stress, a constant stress condition (V_{DS} = 50 V, V_{GS} =

-7 V) was applied over a duration of 3600 s to the gate and drain regions, with the source being grounded. To investigate the temperature dependence under the off-state stress, both devices, having the same gate length of L_G =14 μm, were stressed at constant voltage (V_{DS} = 50 V, V_{GS} = -7 V) for 1 h by increasing the temperature from 298 K to 368 K in steps of 10 K. Figure 3.2 shows critical voltages determined by off-state-step stress condition.

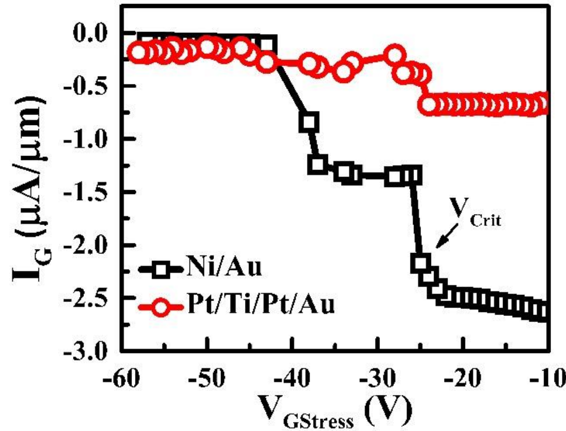


Figure 3.2 : Critical voltages (V_{crit}) of Ni/Au and Pt/Ti/Pt/Au on AlGaN/GaN HEMTs in the range of -10 to -60 V with stepped stresses. The V_{crit} of Ni/Au is about -25 V and that of Pt/Ti/Pt/Au is unspecified for up to -60 V.

The critical voltage of the Ni/Au HEMT, followed by a sudden increase in the gate leakage current, is about -25 V, which results in permanent defect sites at the MS interface. This sudden increase in the gate leakage current can be ascribed to the inverse piezoelectric effect [76]. In contrast, no sudden increase in the gate leakage current is observed up to -60 V in the Pt/Ti/Pt/Au HEMT [77]. To verify the degradation of the SBH from high electrical stress, the forward and reverse leakage currents of the Ni/Au and Pt/Ti/Pt/Au contacts on the AlGaN/GaN HEMTs are evaluated before and after off-state stress application (V_D = 50 V, V_G = -7 V) over a duration of 3600 s. The reverse leakage current of the Pt/Ti/Pt/Au contact after off-state stress application shows a greater reduction than that of the initial device while that of the Ni/Au increases, as shown in Figure 3.3.

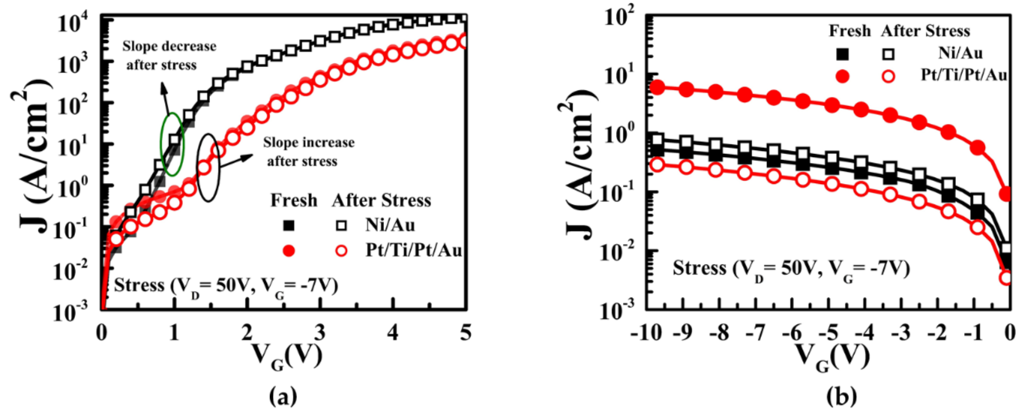


Figure 3.3 : (a)Forward leakage current and (b) Reverse leakage current of Ni/Au and Pt/Ti/Pt/Au on AlGaN/GaN HEMTs before and after off-state stress (V_D = 50V, V_G = -7V) during 3600 s.

It is also interesting to note that the SBHs of the Ni/Au and Pt/Ti/Pt/Au after application of off-state stress decrease from 0.55 to 0.49 eV and increases from 0.46 to 0.69 eV, respectively. This means that the hot carriers under the off-state stress have significantly affect the MS. In fact, the stress condition at room temperature (25°C) depends significantly on the gate voltage and electric field. The metallization schemes for the Schottky contacts on the AlGaN/GaN HEMT must thus be verified for thermal instabilities due to Ga out-diffusion and Au interdiffusion at elevated temperatures. The thermal reliability instabilities for the Ni/Au and Pt/Ti/Pt/Au HEMTs are examined in the temperature range of 298 to 368 K in intervals of 10 K. Figure. 3.4 shows the J-V characteristics of the Ni/Au and Pt/Ti/Pt/Au contacts after application of off-state stress (V_D = 50 V, V_G = -7 V) at different temperatures. The reverse leakage currents of the Ni/Au HEMT before and after off-state stressing at 298 K are not degraded; in fact, the off-state stress with increasing temperature causes greater initial-parameter degradation rather than at room temperature [78] as shown in Figure 3.4 (a), which can easily generate more interface traps. In contrast, the reverse leakage currents of the Pt/Ti/Pt/Au HEMT decrease after off-state stressing at 298 K, with further reduction at 308 K under the same off-state stress conditions.

To see the degradation of the gate current and threshold voltage, the same off-state step stress test is performed in the reliability device (W_g = 50 μm, L_g = 3 μm, L_{sd} = 7 μm) includes the epitaxial structures consist of a 28 nm $Al_{0.25}Ga_{0.75}N$ barrier layer, a 150 nm GaN channel layer, an AlN nucleation layer (10 nm, whose thickness is not shown in the cross-sectional diagram), and a 2.6 μm high-resistance GaN buffer layer depicted in figure 3.4

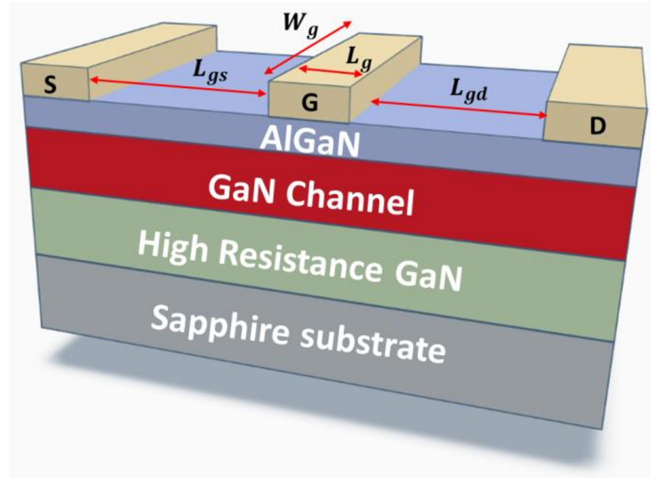


Figure 3.4 : Schematic Diagram of AlGaN/GaN HEMTs

The highest output current (I_{DS}) and the maximum transconductance (G_{max}) were found to be 500 mA/mm (at V_{GS} = 5 V) and 115 mS/mm at V_{DS} = 10 V. From, V_{GS} = 0 V to 2 V, there observed self-heating effect (lowering the output conductance, G_d) of the device at the higher drain voltage (V_{DS} > 5 V).

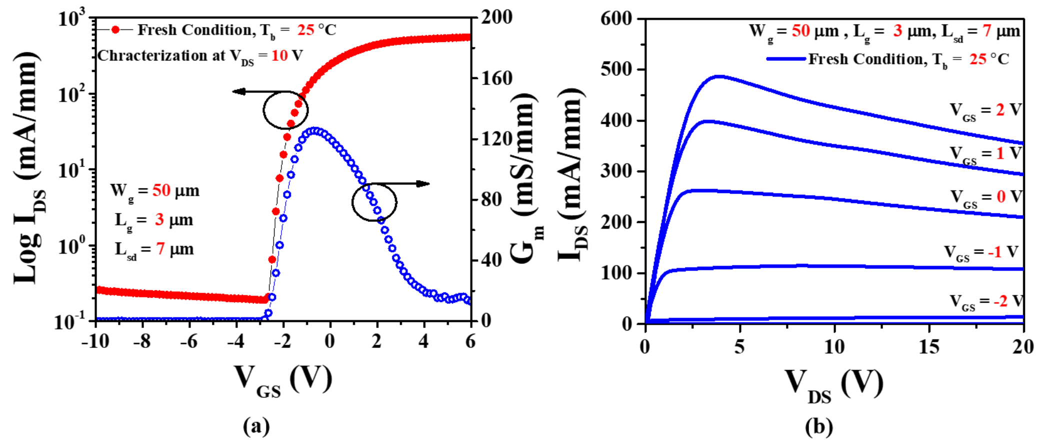


Figure 3.5 : (a) Transfer and (b) Output Characteristics of AlGaN/GaN HEMT at room temperature (25 °C).

3.2 Off-state Stress test

In the Off-state step stress test, gate voltage kept fixed beyond the threshold voltage, V_{GS} = -10 V while source terminal grounded. Drain voltage (V_{DS}) stepped from 10 V to 100 V with 5 V/step and duration for each step was 60s. Figure 3.6 represents the off-state step stress results

where source terminal kept ground and V_{GS} set to -10 V (device's threshold voltage , V_T = -2 V) at room temperature, T_b = 25 °C. Gate current (I_g) decreases up to V_{DS} = 25 V stress around 300 s. After V_{DS} = 25 V step stress, I_g gradually increased and at V_{DS} = 50 V around 800 s stress, it becomes noisy. Figure 3.6 (b) plots the transfer characteristics after stress which indicates that drain current (I_{ds}) decreased and threshold voltage shifted to the positive direction. After 10 V stress, drain current reduces around ΔI_{ds} = 30 mA/mm from fresh condition, ΔV_T = -0.5 V, transconductance reduces ΔG_{max} = 20 mS/mm and off-state gate leakage current increased around 100 mA/mm (shown in inset of Figure 6 (b)). After 50 V stress, ΔI_{ds} = 50 mA/mm from the fresh condition and threshold voltage shifted around ΔV_T = -2.03 V. No changes were observed in the gate leakage current after the initial increase, and with further stress, the threshold voltage did not shift but rather reached a saturation point.

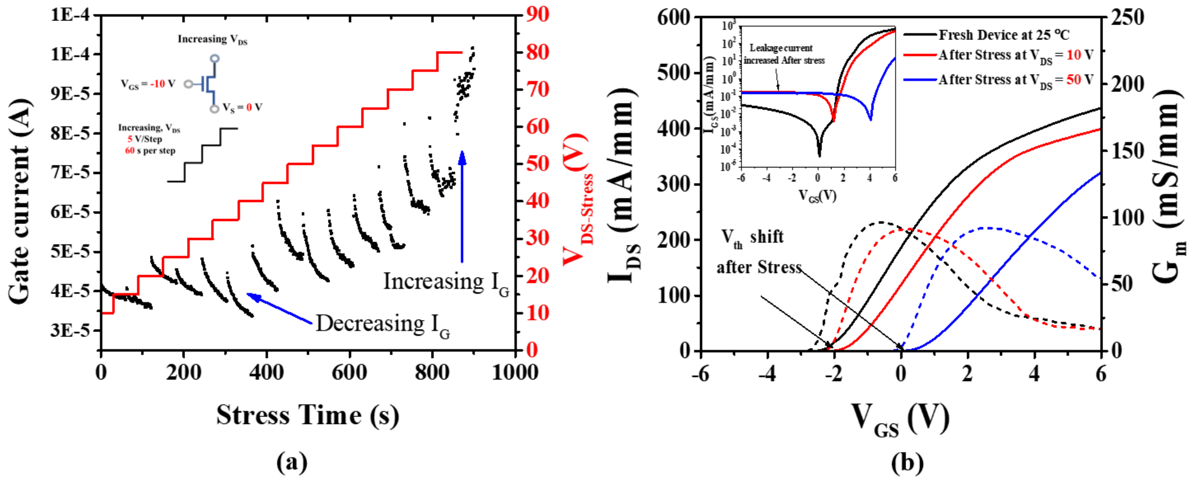


Figure 3.6 (a) Off-step stress test procedure, gate current becomes noisy after V_{DS} = 50 V stress. (b) threshold voltage shift (ΔV_T) and Schottky characteristics (inset) shown after stress.

A positive threshold voltage shift represents electron trapping at the gate and gate-to-drain access region. Under certain voltage conditions, specifically, V_{DS} = 50 V; V_{GS} = -10 V, the gate leakage current exhibited an increase that proved to be permanent. This phenomenon suggests the occurrence of defect generation at the gate-to-drain side, known as lateral breakdown, as the electric field (E_x) is most intense in that region during off-state conditions [17]. Consequently, electrons are injected into the barrier layer (AlGaN) from the gate, resulting in an escalation of the gate leakage current. The saturation of the threshold voltage (V_T) after V_{DS} = 50 V stress can be attributed to trap sites being occupied by electrons, leaving no room for further shifting in that state.

3.3 V_{DS} = 0 V Step Stress test

In V_{DS} = 0 V, step stress test, gate voltage (V_{GS}) increased from -10 V to -100 V at 10 V/step in reverse gate bias condition, while source and drain terminals grounded. This step stress duration was 100s/step. Figure 3.7 (a) demonstrates V_{DS} = 0 V step stress test where the device step stress from -10 V to -100 V while keeping the drain and source terminal ground. From V_{GS} = -10 V stress, gate current (I_g) increases gradually and after V_{GS} = -50 V, gate current reduces and keeps reducing up to V_{GS} = -90 V. After V_{GS} = -100 V, the device breakdown occurred.

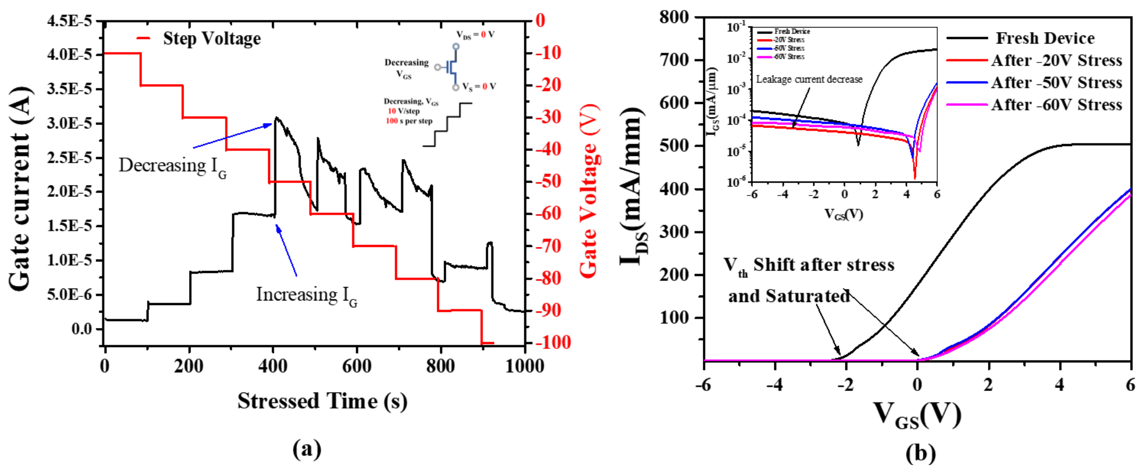


Figure 3.7 (a) Gate leakage current characteristics in V_{DS} = 0 state condition.(b) threshold voltage shift (ΔV_T) and Schottky characteristics (inset) demonstrated where the leakage current decreased after stress.

Figure 3.7 (b) plots the I-V characteristics after and before stress at room temperature. After V_{GS} = -20 V stress, threshold voltage (ΔV_T) shift around -2.0 V and the drain current decreases heavily (ΔI_{DS} = 104 mA/mm). Gate leakage current exhibits a decrease after V_{GS} = -20 V, followed by a slight increase after V_{GS} = -50 V, and subsequently decreases again after V_{GS} = -60 V. The threshold voltage shift reached saturation after the stress at V_{GS} = -20 V. This behavior exhibits similarities to the inverse piezoelectric effect, where the leakage current increases after V_{GS} = -50 V stress but gradually decreases after V_{GS} = -60 V until V_{GS} = -100 V. However, contrary to the inverse piezoelectric effect's predictions, where degradation is observed after the critical voltage and the gate leakage current continuously increases, in this case, after V_{GS} = -60 V stress, the gate leakage current (I_g) decreases, as illustrated in the inset of Figure 3.7 (b).

3.4 High temperature operating life-time (HTOL) test

The most widely employed method for determining the Mean-time-to-failure (MTTF) is through High-Temperature Operating Life (HTOL) tests. The High-Temperature Operating Life (HTOL) test is an accelerated lifetime test that centers on assessing device degradation under specific voltage conditions while subjecting it to stress at three different temperature levels. Following the HTOL test, Mean-Time-to-Failure (MTTF) predictions are made using the Arrhenius model. This model is based on the assumption that the rate of device failures is exponentially related to temperature and can be expressed as follows:

$$\lambda = Ae^{\left(\frac{E_a}{kT}\right)} \tag{3.3}$$

Where, λ is the failure rate, A is a material constant, E_a is the activation energy (a measure of the energy barrier for failure mechanisms), k is the Boltzmann constant, and T is the absolute temperature (in Kelvin).

This equation outlines the connection between temperature and the rate at which the device degrades due to a specific failure mechanism. The semiconductor industry has widely embraced this equation as a guiding principle for overseeing device operation under diverse temperature conditions. The Arrhenius model allows for the determination of an acceleration factor (AF), which relates the failure rate at elevated stress conditions (T_{stress}) to the failure rate at normal operating conditions (T_{normal}):

$$AF = e^{\left(\frac{E_a}{kT}\right)\left(\frac{1}{T_{normal}}-\frac{1}{T_{Stress}}\right)} \tag{3.4}$$

One crucial assumption in this methodology is that failure mechanisms are thermally activated, and the Arrhenius model accurately describes the relationship between temperature and failure rate. The accuracy of MTTF calculations relies on the validity of the acceleration factor and the assumption that failure mechanisms. The accuracy of MTTF calculations relies on the validity of the acceleration factor and the assumption that failure mechanisms under accelerated testing conditions are representative of those under normal operating conditions. The channel temperature (T_{ch}) of the device plays a vital role in determining the activation energy and acceleration factor. Temperature variations can significantly influence device reliability, so precise temperature measurements and control are essential during accelerated testing. Accurate measurement and control of channel temperature are critical, as temperature variations directly impact device reliability and influence the activation energy used in the model.

3.4.1 Channel Temperature determination

Thermal evaluation plays a crucial role in the design, analysis, and assessment of semiconductor devices and circuits, ensuring their proper functioning and reliability [79]. The reliability and power management of compound semiconductor devices largely depends on the junction or channel temperature [80] . At high power densities, the performance of semiconductor devices is hindered by as self-heating, which occurs due to Joule heating [81]. Therefore, the elevated temperature within GaN devices emerges as a prominent concern, posing a significant challenge to their overall reliability [82]. Mitigating self-heating and its associated issues necessitates meticulous attention to device design, layout, material dimensions, as well as effective heat transfer and heat sinking strategies [83]. Numerous researchers are currently conducting both experimental and theoretical investigations on this phenomenon. Jakani et al.[84] measures the channel temperature of GaN HEMTs through thermos-reflectance technique. Bruce M Paine et al.[85] used the gate end-to-end resistance method to measure the channel temperature inside GaN. Kuball et al. [86] demonstrate the importance of Raman thermography to accurate measurement of channel temperature. Gate resistance thermometry measure also performed by Karrame et al. [87]. In terms of modeling, analytical thermal model was established by Li et al. that use conformal mapping method [88]. The industry standard compact model also developed [89, 90]. A wide range of intricate models has been presented, with some rooted in physics while others rely on empirical foundations [91-94]. A channel temperature calculation approach for multiple gate fingers was proposed by Darwish et al. [95]. Masana proposed a gate-angle-related channel temperature for single-gate HEMTs, which involves a substantial number of estimates, multiple components, and a complex model with diverse parameters [96, 97]. Therefore, a compact thermal model is crucial for GaN HEMTs to enable efficient computation and initial investigations. In this study, we have introduced a simplified empirical thermal model utilizing Maclaurin series expansion. To ascertain the precision of the modeled data, we conducted TCAD (Silvaco) simulations and performed a comprehensive comparison between the outcomes of the proposed model, measurement data, and TCAD simulations.

3.4.2 Channel temperature Model

A typical AlGaN/GaN on sapphire HEMTs structure is shown in Fig. 3.4 which has highly localized heat source area ($L_g \times W_g$) under the gate. In all instances, the thickness of the AlGaN barrier layer is considered negligible, with no significant contribution to additional

thermal resistance. Furthermore, a temperature dependent thermal conductivity (*k*) is assumed for all substrates. As temperature rises, the thermal conductivity of numerous semiconductor materials, such as silicon (Si), Gallium Arsenide (GaAs), and Gallium Nitride (GaN), exhibits a decreasing trend. As a requisite outcome, the influence of temperature-dependent thermal conductivity adds an extra temperature elevation that necessitates careful consideration in the thermal analysis of GaN-based electronics. The non-linear heat conduction equation, which accounts for temperature-dependent thermal conductivity, can be solved effectively using Finite Element Analysis (FEA) models. Kirchhoff's transformation, as a general approach, transfers nonlinearity from the heat-flow equation to the boundary conditions. To address steady-state conduction heat transfer problems with temperature-dependent thermal conductivity, Kirchhoff introduced a function *U* as the foundation for an integral transform as follows [98]:

$$U = K\{T\} = \int^{T} k(\tau) d\tau \tag{3.5}$$

The lower limit of this integral can be any value. The fundamental demonstration of the equation represents,

$$\frac{dU}{dT} = k \tag{3.6}$$

further denoted by the Calculus divergence theorem and chain rule of differentiation which modified the non-linear conduction equation in the following form:

$$\nabla.(k\nabla T) = 0 \tag{3.7}$$

By transforming the above equation into the Linear Laplace's form

$$\nabla^2 U = 0 \tag{3.8}$$

The inverse Kirchhoff transform can be used to ascertain the real temperature,

$$T = K^{-1}\{U\} \tag{3.9}$$

once the functional version of the thermal conductivity relationship $k = k(T)$ has been determined. The most widely recommended Kirchhoff's transform is given by,

$$\theta = \frac{1}{k_0} \int_0^{T} k(\tau) d\tau \tag{3.10}$$

Theta (θ) is associated to Kirchhoff's function $U= k_0\theta$ and k_0 is the thermal conductivity of the medium estimated at $T=0$. This non-linear equation is governed by linear Laplace's equation,

$$\nabla^2\theta=0 \tag{3.11}$$

Joyce [98] clarified that the apparent temperature can be presented as

$$\theta = T_0 + \frac{1}{k_0}\int_{T_0}^{T} k(\tau)d\tau \tag{3.12}$$

Where T_0 is the boundary temperature of heat-sink in the context of electronic thermal spreading complications. If the temperature difference between the Channel and the Substrate temperature (bottom) of the chip presented by ΔT then Kirchhoff's transform rewritten as

$$\Delta T = \frac{1}{k_0(T)}\int_{T_0}^{T} k(T^{'})dT^{'} \tag{3.13}$$

Where $k(T_0)$ is the thermal conductivity appraised at the backside contact temperature T_0. Hence one closed form expression for channel temperature depicted by Canfield et al. [99] using Kirchhoff's transformation,

$$\frac{\Delta T}{T_0} = \frac{1-(1-\frac{P_{diss}}{4P_0})^4}{(1-\frac{P_{diss}}{4P_0})^4} \tag{3.14}$$

Where, P_{diss} represents power dissipation and P_0 is denoted by,

$$P_0 = \frac{\pi k(T_{sub})W_g T_{sub}}{\ln(\frac{8t_{sub}}{\pi L_g})} \tag{3.15}$$

If the thermal conductivity is not constant, then the above equation can be modified into the following formula by inserting $k(T) = k_{T_0}\left(\frac{T}{T_0}\right)^{-\alpha}$, where α is constant, k_{T0} is the conductivity at temperature T_0. The equation (3.15) can be expressed as below:

$$P_0 = \frac{\pi k_{T_0} W_g (T_{sub})^{1-\alpha} T_0^{\alpha}}{\ln(\frac{8t_{sub}}{\pi L_g})} \tag{3.16}$$

Where P_{diss} is the power dissipation, L_g is the gate length, W_g is the gate width, and t_{sub} is the substrate thickness. To obtain a clearer perspective, the above equation can be represented as

$$T_{ch} = \left[\frac{1-(1-\frac{P_{diss}}{4P_0})^4}{(1-\frac{P_{diss}}{4P_0})^4} T_{sub} \right] + T_{sub} \tag{3.17}$$

This model equation overestimates the channel temperature (T_{ch}) mentioned in our previous work [100]. Therefore, we modified $(1-\frac{P_{diss}}{4P_0})^{-4}$ this term into Maclaurin series. The Maclaurin series can be stated as,

$$f(x) = f(0) + f'(0)x + \frac{f''(0)}{2!}x^2 + \frac{f'''(0)}{3!}x^3 + ... + \frac{f^{(n)}(0)}{n!}x^n \tag{3.18}$$

Using the above equation, the term $(1-\frac{P_{diss}}{4P_0})^{-4}$ can be expressed as follows:

$$= \frac{P_{diss}}{P_0} + \frac{5}{8}\left(\frac{P_{diss}}{P_0}\right)^2 + \frac{5}{16}\left(\frac{P_{diss}}{P_0}\right)^3 + \frac{35}{256}\left(\frac{P_{diss}}{P_0}\right)^4 \tag{3.19}$$

The higher terms (3rd and 4th terms) can be ignored. The thermal model or channel temperature equation can be expressed as below:

$$T_{ch} = \gamma\left(\frac{P_{diss}}{P_0}\right)^2 + \frac{P_{diss}}{P_0}T_{sub} + T_a \tag{3.20}$$

Where, γ in the polynomial coefficient, T_a is the ambient temperature. The proposed closed-form empirical expression for channel temperature will be subjected to verification using a dataset obtained from measurements and TCAD Silvaco simulations.

To estimate the channel temperature without direct measurement, we employed the channel temperature equations in our modeling approach, incorporating all relevant practical parameters. In our modeling the following parameters are utilized : substrate thickness, $t_{sub} = 430$

µm, substrate thermal conductivity, k_{sub} = 49(27/T_{sub}) W/m-C, gate length, L_g = 3 µm, T_0 = 25 °C, and gate width, W_g = 50 µm. Table 3.1 represents the calculation of the channel temperature using our modeling equation. We considered temperature dependent thermal conductivity for calculating the value of P_o.

Table 3.1 : Channel temperature calculation through the proposed methodology.

P_0	$P_{diss}(W)$	P_{diss}/P_0	$(P_{diss}/P_0)^2$	$\gamma(P_{diss}/P_0)^2$ $\gamma = 0.63$	$\gamma(P_{diss}/P_0)^2 + T_{sub}(P_{diss}/P_0) + T_a$ $T_a = 25$ °C
0.1422	0.006731	0.047335	0.002241	0.001412	26.18478
0.1358	0.018139	0.133571	0.017841	0.01124	28.35053
0.1305	0.030022	0.23005	0.052923	0.033341	30.78459
0.126	0.040502	0.32144	0.103324	0.065094	33.10111
0.122	0.051499	0.422123	0.178188	0.112258	35.66533
0.1186	0.062468	0.526707	0.277421	0.174775	38.34246
0.1155	0.073554	0.636827	0.405548	0.255496	41.17617
0.1128	0.084126	0.745793	0.556208	0.350411	43.99525
0.1103	0.095895	0.869397	0.755851	0.476186	47.21111
0.1081	0.106325	0.98358	0.96743	0.609481	50.19898
0.106	0.117547	1.108929	1.229724	0.774726	53.49796
0.1041	0.12842	1.233617	1.52181	0.95874	56.79916
0.1023	0.139581	1.364428	1.861664	1.172848	60.28355
0.1007	0.151273	1.502214	2.256648	1.421688	63.97705
0.0991	0.161715	1.631831	2.662874	1.677611	67.4734
0.0977	0.172068	1.761187	3.101781	1.954122	70.9838
0.0963	0.182926	1.899538	3.608244	2.273194	74.76164
0.0951	0.193719	2.037003	4.149382	2.614111	78.53919
0.0938	0.204696	2.18226	4.762259	3.000223	82.55673
0.0927	0.215651	2.326327	5.411797	3.409432	86.5676
0.0916	0.22665	2.474345	6.122383	3.857101	90.71573
0.0896	0.237438	2.649972	7.022352	4.424082	95.67338
0.0887	0.247614	2.79159	7.792973	4.909573	99.69931

To validate our model data regarding channel temperature, we conducted both measurements and TCAD simulations, which are discussed in the following section.

3.4.3 Channel temperature determination by Electrical Method

Figure 3.5 (a) and (b) plot the transfer and output characteristics of sapphire substrates based HEMTs respectively. A distinct observation emerges from the data, indicating that the sapphire substrate exhibits a more pronounced negative differential resistance as the gate voltage increases, primarily due to the influence of device self-heating effects. Self-heating phenomena occur when the power added to the device generates heat that is inadequately dissipated, leading to the device operating at the substrate's ambient temperature. When the drain bias is high, self-heating effects enhance the device's lattice temperature and degrade physical properties, including mobility (μ (m^2/V · s)) and carrier saturation velocity (V_{SAT}) [101-104] The mobility decreases with increasing temperature as $(1/T)^{2.3}$, with a resulting decrease in DC and RF

performance [105]. We have followed the [106] to determine the channel temperature by electrical method. Figure 3.8 represents the comparison between channel temperature measurement for different gate voltages (V_{gs} = 2 V, 1 V and 0 V).

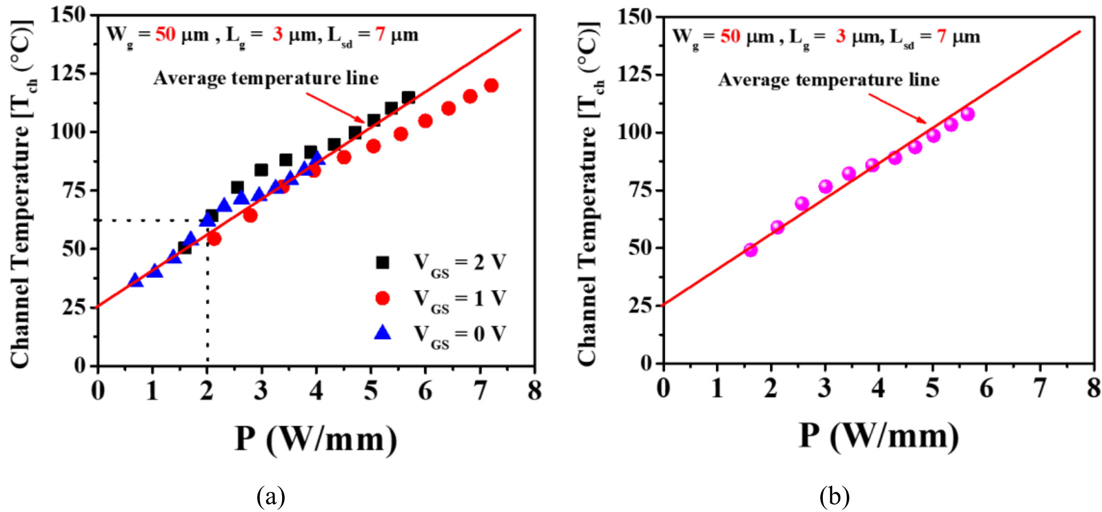


Figure 3.8 : Channel temperature measurement for three different gate voltages and average channel temperature line plotted for measurement data.

3.4.4 TCAD Simulation of Channel Temperature

In the context of TCAD (technology computer-aided design) simulation, specific mesh settings were defined for precise modeling. The mesh width was established at 50 microns, with the primary spacing in the x-plane set at 0.25 µm for the source and drain metal regions. Similarly, the mesh spacing for the source-to-gate (L_{sg}) and gate-to-drain (L_{gd}) regions was set at 0.25 µm. In the y-plane, the meshing ranged from 0 to 0.50 µm, with a spacing of 0.1 µm. This area covered the "air" region (region number 1). Beyond that, the AlGaN barrier (region number 2) extended from 0.50 to 0.520 µm, with an aluminum composition of 0.25% and a mesh spacing of 0.01 µm.

The GaN channel (region number 3) spanned from 0.520 to 0.670 µm, also with a mesh spacing of 0.01 µm. The buffer region (region number 4) ranged from 0.670 to 3.070 µm and was uniformly doped with carbon (p-type), maintaining a mesh spacing of 0.01 µm. The AlN nucleation layer (region number 5) was extremely thin, from 3.070 to 3.018 µm. Finally, the sapphire substrate (region number 6) was in the range from 3.180 µm to the end of the device. Three electrodes were defined as source (y.min = 0.40 µm, y.max = 0.65 µm), drain (y.min = 0.40 µm, y.max = 0.65 µm), and gate (y.min = 0.40 µm, y.max = 0.50 µm). The work functions for these electrodes were specified as 5.20 eV, 4.0 eV, and 4.0 eV for gate, source, and drain, respectively.

In the simulation process, the high-field mobility was computed utilizing the Farahmand modified Caughey–Thomas (FMCT) and GANSAT models, while the low-field mobility was determined using the Albrecht model. Various physical models, including Schottky–Read–Hall (SRH), Fermi–Dirac statistics (FLDMOB), CONMOB, Fermi, and KP, were considered in the model definition. The polarization parameter was set to 0.952.

To account for self-heating effects, a lattice temperature model (lat. temp) was incorporated for channel temperature estimation in TCAD modeling, where the substrate is stated as "thermalcontact num = 1", with the specific region defined as region number 5, external temperature (ext.temp) set as 300 K, and adjusted thermal resistance (R_{th} = 1/α). Additionally, the Selberherr impact ionization model (Impact selb) parameters, namely an1, an2, bn1, bn2, ap1, ap2, bp1, and bp2, were set to specific values, namely 2.9×10^8, 2.9×10^8, 3.4×10^7, 3.4×10^7, 2.9×10^8, 2.9×10^8, 3.4×10^7, and 3.4×10^7, respectively. These parameters are essential for accurately modeling the device's behavior and performance in the simulation environment.

Figure 3.9 illustrates the TCAD simulation results for the device with W_g = 50 µm, L_g = 3 µm, and L_{sd} = 7 µm on the sapphire substrate for three different drain voltages V_{DS} = 10 V, 15 V and 20 V at fixed gate bias V_{GS} = 0.5 V. Localized hot spot is increasing while increasing the power at high voltage condition. For different drain voltages V_{DS} = 10 V, 15 V and 20 V the peak channel temperature showing 54 °C, 66 °C and 77 °C inside the channel (cross-section AA') respectively shown in Figure 3.10. While increasing drain voltage from V_{DS} = 10 V to V_{DS} = 20 V power dissipation is also increased as 4.2 W/mm to 7.1 W/mm at V_{GS} = 2 V.

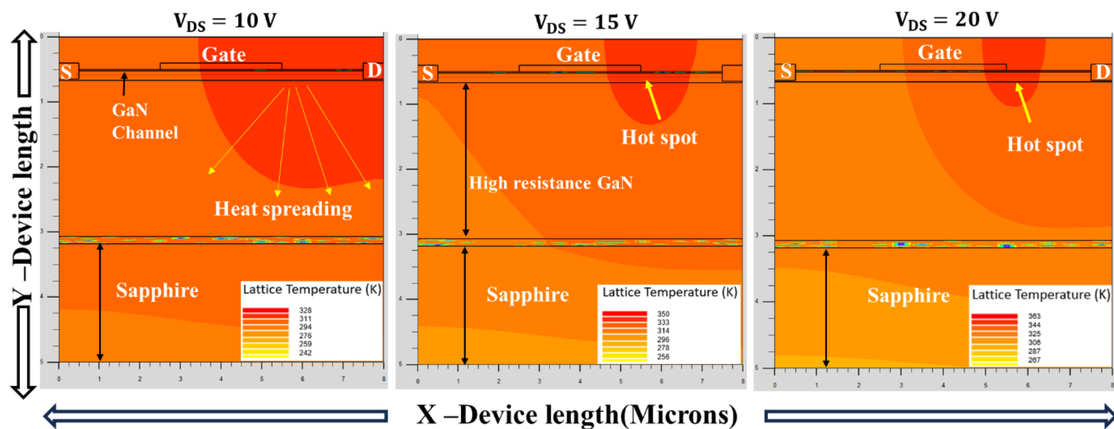


Figure 3.9 : TCAD simulation of the AlGaN/GaN, same structure of the experiment showing the lattice temperature change depending on the bias condition from V_{DS} = 10 V to V_{DS} = 20 V.

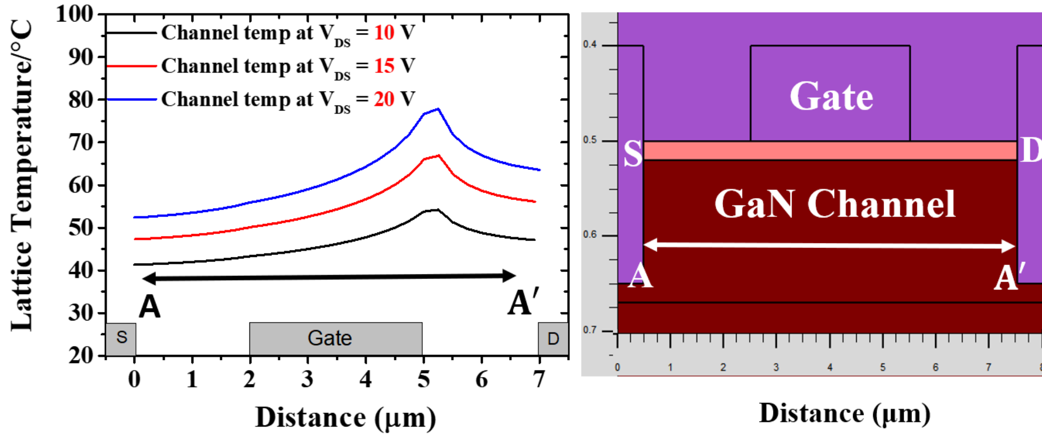


Figure 3.10 : Channel temperature inside the GaN channel represented by the cross-section AA' .

Figure 3.11 demonstrates a close agreement between the TCAD simulation and measurement results of output characteristics.

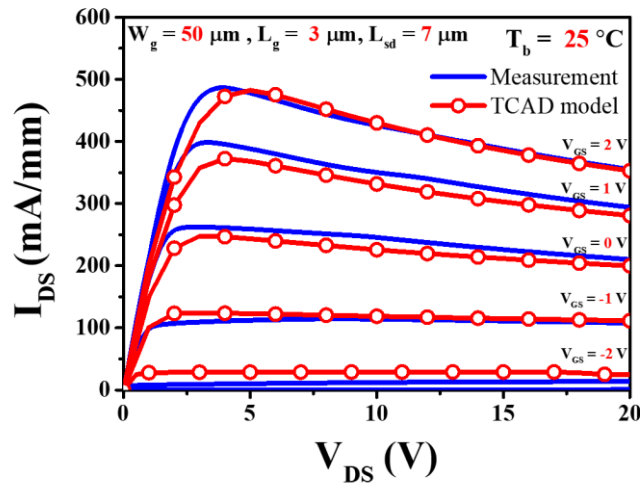


Figure 3.11 :TCAD model simulation and measurement results (output characteristics).

Figure 3.12 plots the channel temperature from both TCAD simulation and our presented model. The models, taking into account the temperature-dependent thermal conductivity of the sapphire substrate, clearly exhibit non-linearity in the high-power dissipation region (starting from 4 W/mm).

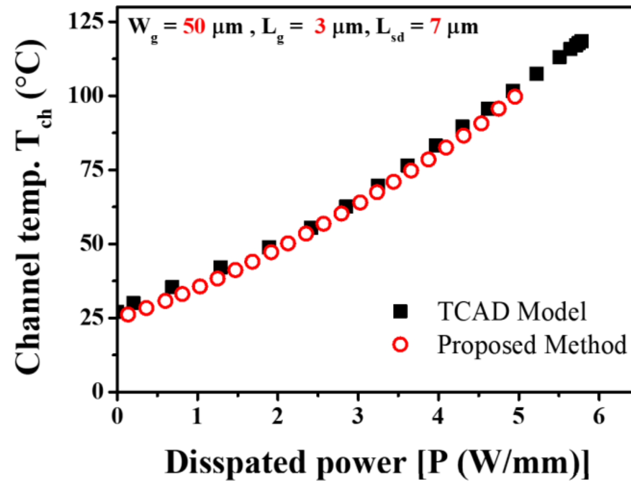


Figure 3.12 : TCAD model simulation and our proposed model results show close agreement.

A close agreement between our model and TCAD simulations is evident, as depicted in Figure. 3.13. The figure presents the overall channel temperature data obtained from measurements, TCAD simulations, and our presented model. Our model aligns perfectly with both the measurement results and the TCAD simulation.

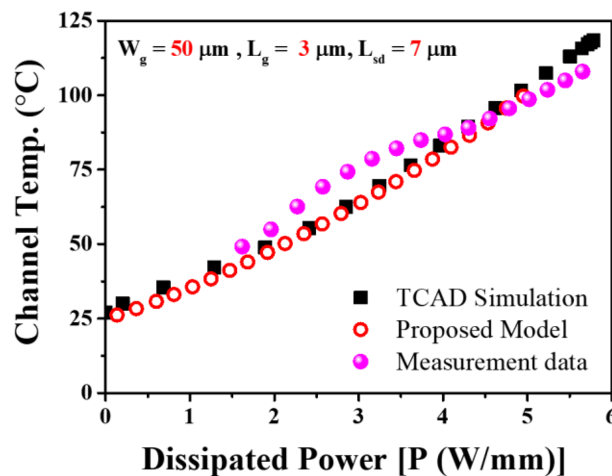


Figure 3.13 : Measurement data and TCAD simulation shows very close agreement to our proposed model data.

After determining channel temperature precisely, the HTOL test is conducted into various stress conditions. In HTOL test, stress voltage condition was chosen to V_{DS} = 10 V, 15 V and 20 V. At each voltage stress condition, the device stressed at three base plate temperatures, T_b = 150 °C, 175 °C and 190 °C. Corresponding junction/channel temperature was estimated at T_{ch} = 220 °C, 245 °C and 260 °C for above mentioned base plate temperature (T_b = 150 °C,

175 °C and 190 °C) respectively by electrical measurement[58]. We considered average channel temperature data (shown in red line) for calculation. For one set of stress voltage conditions, a minimum of 5 devices were subjected to stress for each temperature condition. The stress duration kept up to more or less than 200 hrs. depending on the 15% degradation of I_{dmax} (defined at V_{GS} = 1 V, V_{DS} =5 V) of the device. At the same time, transconductance (G_{max}), threshold voltage shift (ΔV_T), on-resistance (R_{on}) and gate leakage current (I_{g_leak}) were reported to observe the degradation characteristics.

3.4.5 TCAD Simulation of Electric Field and potential

Figure 3.14 shows the output and transfer characteristics (at V_{DS} = 10 V) of the device at T_b = 25 °C. The graph depicts three distinct bias zones: the on-state (V_{GS} > 1.0 V), the semi-on state (-2.0 V to 0.5 V) and the off-state (< -2.0 V). Notably, the off-state condition exhibits negligible self-heating effects, while both the semi-on state and full on-state regions demonstrate noticeable self-heating effects at higher drain voltages (> 20 V).

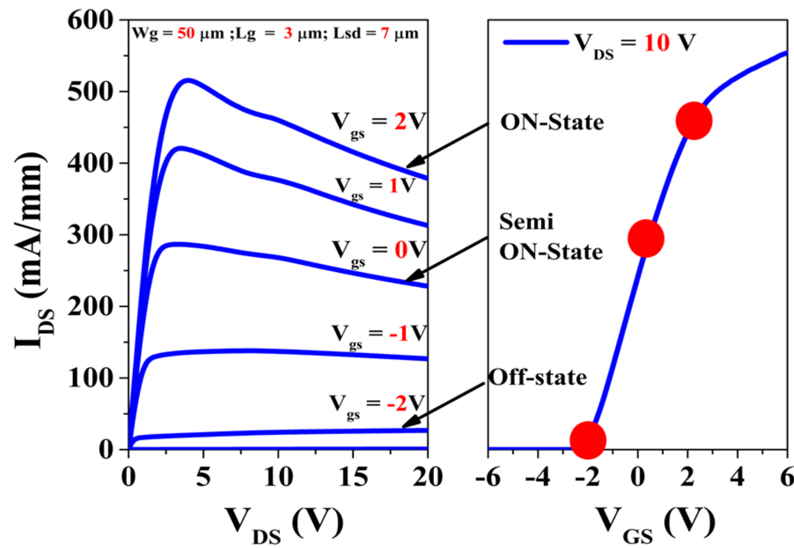


Figure 3.14 : Stress zone (ON-state, Semi on-state and off-state) defined in the output and transfer characteristics of the device.

At constant power dissipation, P = 2 W/mm, devices were stressed at V_{DS} = 10 V, 15 V and 20 V separately fixing the drain current by adjusting the gate voltage. Figure 3.15 presents the results of silvaco TCAD simulations for the devices at three distinct drain voltages. As the drain voltage (V_{DS}) increases from 10 V to 20 V, the electric field potential also experiences a corresponding increase.

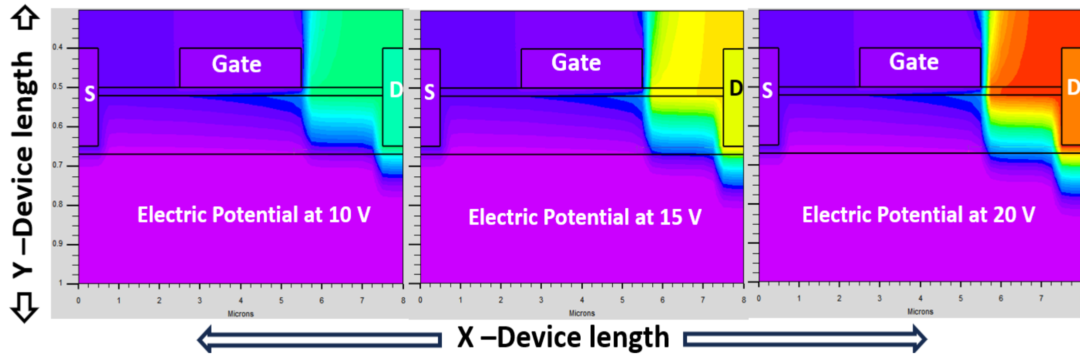


Figure 3.15 : Electric field potential simulation of the device depending on the stress voltage.

The simulation of the electric field (gate to drain region) is depicted in Figure 3.16 , where the highest electric field calculated 2.03 MV/cm for V_{DS} = 20 V, 1.78 MV/cm for V_{ds} = 15 V and 1.50 MV/cm for V_{DS} = 10 V.

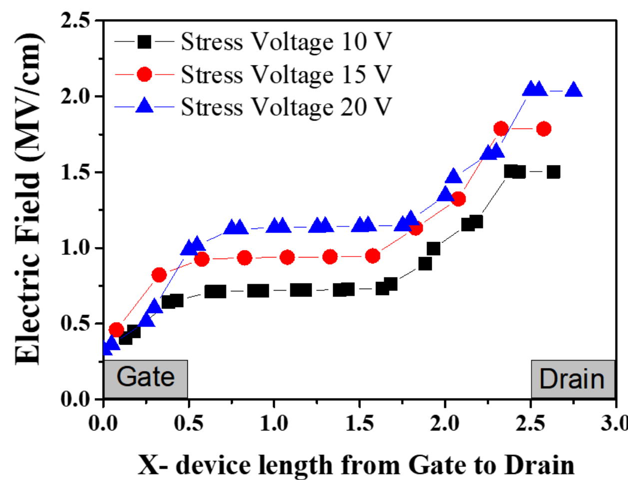


Figure 3.16 : Electric field simulation in different stress voltage condition.

In Figure 3.10, the TCAD simulation displays the channel temperature of the device. The cross-sectional region (AA') in the schematic represents the GaN channel, and it is observed that the peak channel temperature occurs at the gate edge of the drain region. At T_b = 25 °C and a fixed gate voltage of V_{GS} = 0.5 V, the peak channel temperature was estimated to be 54 °C, 66 °C, and 77 °C for drain voltages (V_{DS}) of 10 V, 15 V, and 20 V, respectively. The difference between the peak channel temperatures at V_{DS} = 10 V and V_{DS} = 20 V was approximately 23 °C. During the experiment, the channel temperature was maintained at the same level across all stress levels by adjusting the gate voltage.

3.4.6 Basic degradation parameter analysis after stress

Figure 3.17 (a), (b), and (c) depict the degradation of I_{dmax} (maximum drain current) for the device under three different stress voltage conditions, up to 15% deterioration, at three distinct base plate temperatures. Under the V_{DS} = 10 V stress condition, the device exhibited a gradual degradation trend and sustained for approximately 150 hrs. at T_b = 175 °C. When subjected to higher stress conditions with V_{DS} = 15 V and a lower base temperature (T_b = 150 °C), the device experienced a gradual degradation up to 100 hrs., followed by a period of stability (lower degradation) for 300 hrs., and then a sudden degradation after 300 hrs. until 335 hrs.

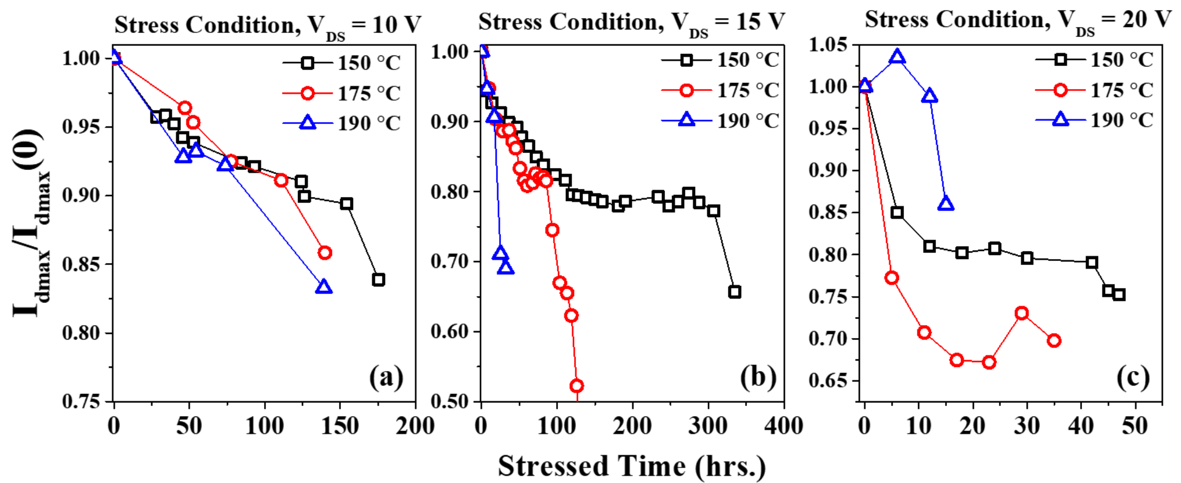


Figure 3.17 I_{dmax} degradation at three channel temperature for the stress voltage, V_{DS} = 10 V, V_{DS} = 15 V and V_{DS} = 20 V.

On the other hand, at T_b = 175 °C under the same stress condition (V_{DS} = 15 V), an abrupt degradation occurred after 100 hrs., leading to device burnout. At high temperatures, specifically T_b = 190 °C, the device experienced a very short operational lifespan of less than 35 hrs. At high stress voltage conditions (V_{DS} = 15 V) and low T_b = 150 °C, the device demonstrated gradual degradation up to 10 hrs., followed by stability, and finally burnt out after 47 hrs. Furthermore, at high temperature (T_b = 190 °C), I_{dmax} initially increased up to 6 hrs. and then gradually degraded over 15 hrs.

Figure 3.18 13 illustrates a comparison of the Idmax degradation at three distinct drain voltages (V_{DS} = 10 V, 15 V, and 20 V) under a specific base plate temperature (T_b = 175 °C). As previously mentioned, the plot shows an abrupt degradation after 100 hrs. for V_{DS} = 15 V.

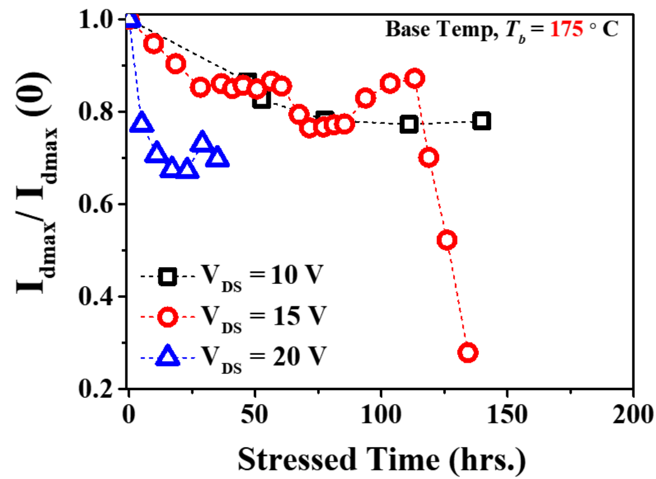


Figure 3.18 I_{dmax} **degradation of different stressed voltage at base plate temperature 175 °C.**

Moving on to Figure 3.19, it displays the G_{max} degradation at the same base plate temperature (Tb = 175 °C). Under a lower stress voltage (V_{DS} = 10 V), G_{max} exhibits gradual degradation, whereas for higher stress voltages (V_{DS} = 15 V and 20 V), a sudden degradation is observed.

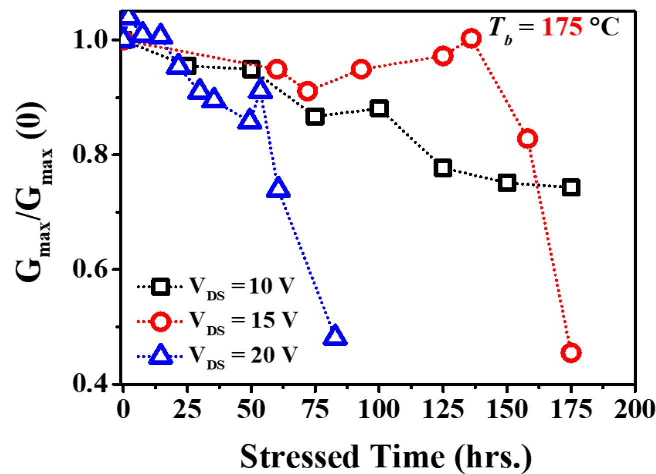


Figure 3.19 G_{max} **degradation of different stressed voltage at base plate temperature 175 °C**.

Figure 3.20 presents a comparison of the threshold voltage shift (ΔV_T) at different stress voltages. At V_{DS} = 10 V, ΔV_T shows a negative shift, approximately -0.33 V (normalized value). For V_{DS} = 15 V, there is negligible ΔVT shift, while for V_{DS} = 20 V, ΔV_T initially experiences a negative shift, recovers after 50 hrs., and subsequently becomes more negative, reaching ΔV_T = -0.13 V (normalized value).

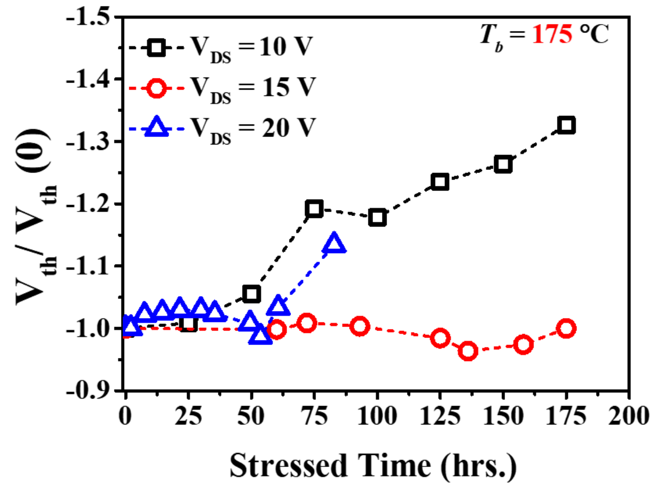


Figure 3.20 : Threshold voltage shift (*ΔV*$_T$) of different stressed voltage at base plate temperature 175 °C.

Figure 3.21 (a) presents a comparative analysis of the On-resistance (R_{on}) at Tb = 175 °C. Under low stress voltage conditions (V_{DS} = 10 V), R_{on} exhibited a 2.5-fold increase after 80 hrs. of stress. For medium stress voltage (V_{DS} = 15 V), R_{on} increased by a factor of 2.0 after 125 hrs. of stress, while at higher stress (V_{DS} = 20 V), R_{on} initially increased 1.6 times after 17 hrs. of stress and then reduced to 1.4 times after 35 hrs. of stress.

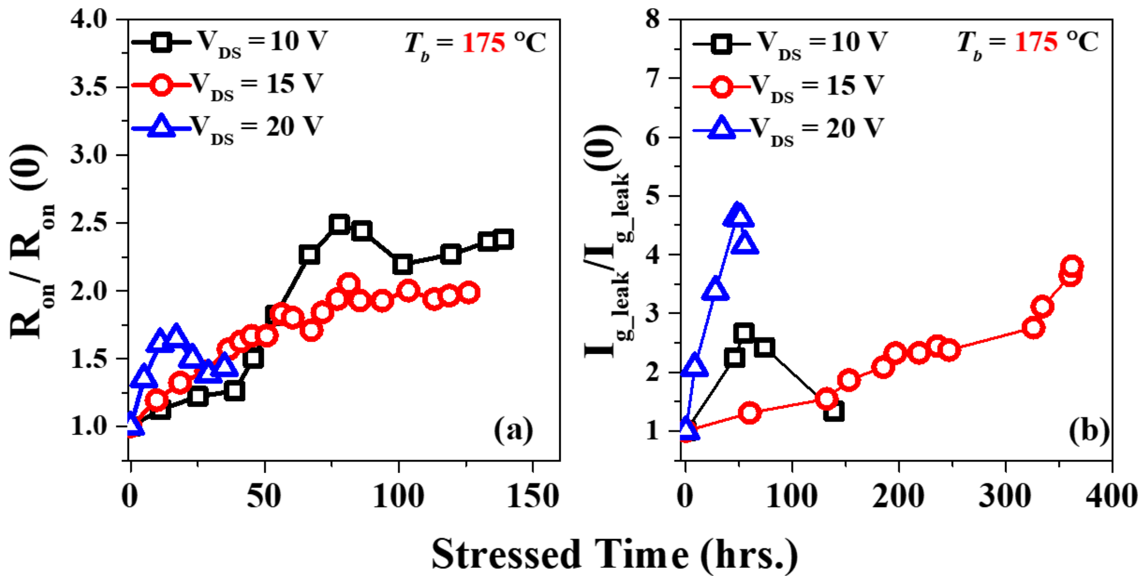


Figure 3.21 (a) On-resistance (R_{on}) and (b) gate leakage current (I_{g_leak}) degradation at T_b =175 °C respectively.

Table 3.2 : Estimation of the activation energy (E_a) and voltage acceleration factor (γ) at different stress condition and different temperature.

Stress Voltage (V)	**Failure time (hrs.) at the base plate temperature (T_b)**			
	150 °C	175 °C	190 °C	Activation Energy (E_a) eV
10	166	140	139 ⇨	0.32
15	138	110	32	0.47
20	52	35	15	0.68
	⇩			
Voltage Acceleration factor (γ) V^{-1}	0.09	0.13	0.16	

Moving on to Figure 3.21 (b), it depicts a comparison of the leakage current (I_{g_leak}) defined at V_{DS} = 10 V and V_{GS} = -10 V. At V_{DS} = 20 V, the leakage current increased more than 4 times higher than its initial value, whereas at V_{DS} = 10 V, I_{g_leak} initially increased up to 2.5 times of the initial value after 55 hrs. of stress, and then it recovered after 139 hrs. Under medium stress (V_{DS} = 15 V) conditions, I_{g_leak} gradually increased and reached 3.8 times its initial value after 362 hrs. of stress, just before the device failure. A comprehensive summary of the experiment is provided in Table 3.2. Table 3.2 presents the results obtained under various stress voltage conditions, where the activation energy (E_a) is determined using the Arrhenius method for three distinct base plate temperatures. Additionally, the voltage acceleration factor (γ) is calculated for each base plate temperature and three different voltage conditions.

The accurate estimation of the channel temperature (T_{ch}) holds significant importance in calculating the mean-time-to-failure (MTTF) of the devices. In Figure 3.22 (a), the MTTF values are plotted against the channel temperature. The extrapolated results reveal distinct MTTF values at T_{ch} = 150 °C for each stress voltage condition; specifically, MTTF is estimated to be 272 hrs. at low stress voltage (V_{DS} = 10 V), 191 hrs. at V_{DS} = 15 V, and 146 hrs. at V_{DS} = 20 V. Moreover, the activation energy increases from 0.32 eV to 0.68 eV with the increment in stress voltage.

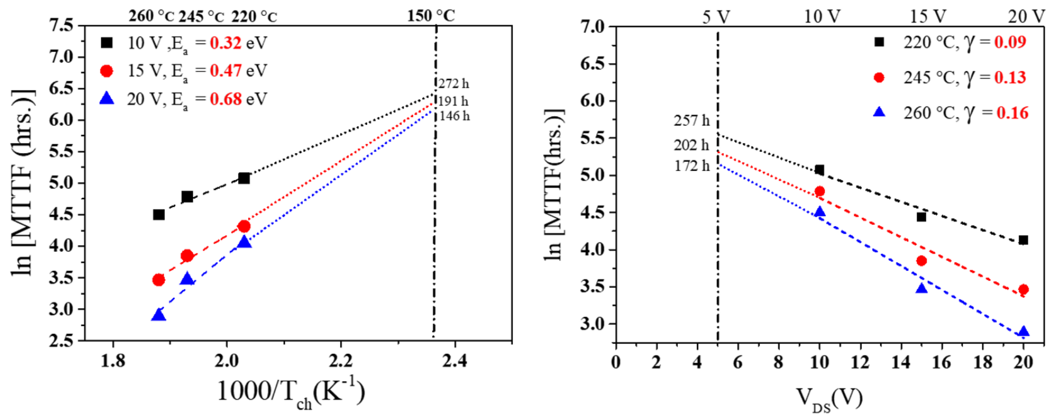


Figure 3.22 (a) MTTF values determined by 3-temperature DC method (Arrhenius) and (b) voltage acceleration factor (*γ*) estimated for three channel temperatures

In Figure 3.22 (b), the MTTF values are plotted against the stress voltages for three different stress voltage conditions, with each specific channel temperature. The voltage acceleration factor (γ) is calculated as 0.09 V^{-1} for T_{ch} = 220 °C, 0.13 V^{-1} for T_{ch} = 245 °C, and 0.16 V^{-1} for T_{ch} = 260 °C. Extrapolated MTTF values are estimated for 5 V at each channel temperature, showing 172 hrs. at higher channel temperature and 257 hrs. at lower channel temperature. Furthermore, the voltage acceleration factor (γ) increases from 0.09 V^{-1} to 0.16 V^{-1} with the rise in channel temperature from 220 °C to 260 °C, respectively.

In Figure 3.23, the MTTF values are determined to be 2.2×10^4 hrs., 1.38×10^4 hrs., and 1.16×10^4 hrs. for three distinct stress voltage conditions at a channel temperature of 65°C. The presence of different activation energy states suggests that AlGaN/GaN devices exhibit multiple degradation mechanisms. Specifically, at stress voltage V_{DS} = 10 V, the degradation mechanism is related to a diffusion process[61], while the values of 0.47 eV and 0.68 eV are closely associated with hot-electron degradation effects.[62]

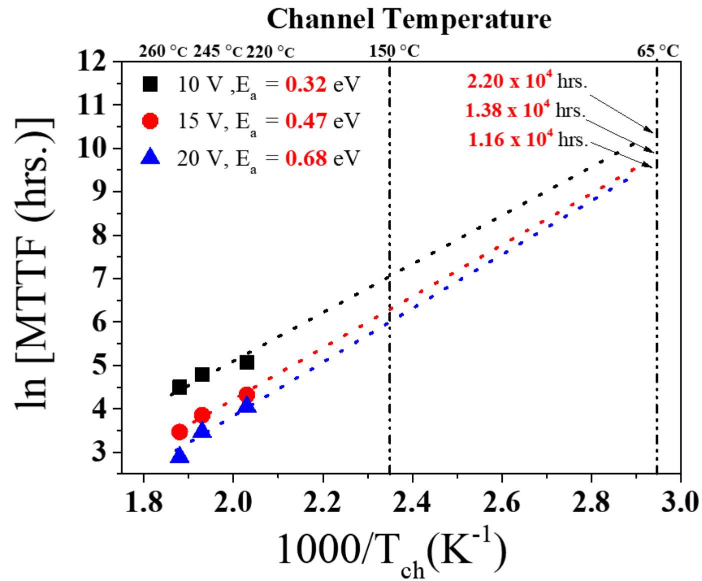


Figure 3.23 MTTF values are determined for long time projection at T_{ch} = 65 °C.

Figure 3.24 provides a detailed examination of the combined voltage and temperature effects. The MTTF values decrease as both voltage and temperature increase. It is important to note that predicting MTTF values based solely on one stress voltage is challenging. Therefore, for an accurate estimation of MTTF, it is necessary to consider both the effects of voltage and temperature.

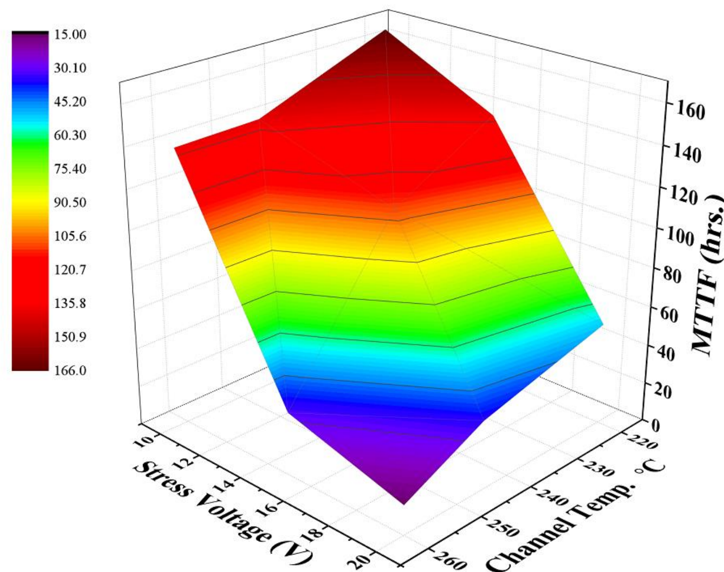


Figure 3.24 Combined effect of voltage and channel temperature for better prediction of MTTF.

3.5 Summary

In this chapter, we have discussed an in-depth investigation into the impact of both activation energy (E_a) and voltage acceleration factor (γ) in the lifetime test of AlGaN/GaN HEMTs. We found that the degradation mechanism cannot be fully explained by solely determining the activation energy, as the failure mechanism in AlGaN/GaN HEMTs significantly depends on the voltage bias point or the electric field. Specifically, at high voltage, the influence of high activation energy dominates, whereas at low voltage, the effect of low activation energy prevails. Consequently, considering the combined effect of stress voltage and channel temperature becomes crucial for accurately determining the Mean Time To Failure (MTTF) values in terms of reliability prediction for AlGaN/GaN devices intended for microwave and RF applications.

Chapter 4

Impact of Electric Field Stress on the reliability

In the previous chapter, we discussed the importance of combined acceleration factors in determining MTTF. We explored the degradation of fundamental parameters under various voltage and temperature conditions. Additionally, we emphasized the significance of precise channel temperature prediction for accurately measuring MTTF values. In this chapter, we will examine how different electric field/ voltage stress conditions impact MTTF values.

4.1 Previous research and literature summary

The mean time to failure (MTTF) serves as a critical parameter in assessing the longevity of devices within the context of long-term reliability. Subsequently, the mean time to failure (MTTF) can be extrapolated from the heightened test temperature to the standard operational temperature, typically hovering around 150 °C for gallium nitride (GaN) devices [107, 108]. In terms of reliability categories, long-term reliability (around 1000 h according to JEDEC standard) at a three-temperature DC test is most used to determine device reliability [109]. Conducting measurements across various junction temperatures (at least three temperatures) facilitates the determination of activation energies (E_a) through the application of the Arrhenius equation. Long-term high-power 50 V DC stress was induced on L_g = 0.5 µm devices with an output current of 150 mA/mm (7.5 W/mm) for a duration of 816 h at channel temperature T_{ch} = 280 °C, 300 °C, and 330 °C [110]. The initial drop in output drain current was observed at 24 h, and the period of stability was around 100–200 h. Beyond this point, the output current relative to time significantly decreased. After a comprehensive physical failure analysis, the emergence of crystallographic defects was ascertained within the entirety of the gate width in the AlGaN layer. This occurrence can be attributed to the manifestation of the inverse piezoelectric effect [111, 112]. However, the analysis did not yield an estimation of the mean time to failure (MTTF).

The failure mechanism analysis of GaN-based HEMTs involves short-term reliability studies (<24 h), as conducted by various research groups [113, 114]. Notably, hot-electron degradation has been well established in GaAs-based HEMTs, and similarly, the hot-electron effect remains a predominant degradation mechanism in GaN HEMTs. The aforementioned study investigated the hot-electron effect through DC short-term tests (<150 h) across diverse HEMT structures. The electroluminescence (EL) intensity exhibited a non-monotonic 'bell-shaped' trend when correlated with V_{GS} while maintaining the V_{DS} constant. Furthermore, a long-term accelerated test was conducted, spanning up to 3000 h, on a specific device at distinct bias points ($V_{GS} = 0$ V, $V_{DS} = 6$ V, (on state); $V_{GS} = -9$ V, $V_{DS} = 32$ V (off state); $V_{GS} = -4$ V, $V_{DS} = 25$ V (semi-on state)). Notably, under the semi-on state condition, a substantial degradation in transconductance (g_m) was observed compared with the other conditions, indicating the presence of the hot-electron effect within the channel. In spite of a thorough examination of the degradation mechanism, the evaluation did not result in the computation of the mean time to failure (MTTF).

Numerous additional research groups have undertaken investigations involving three-temperature DC accelerated Arrhenius test aging, from which activation energies have been deduced [115]. High temperature operating (HTO) tests were conducted by subjecting the devices to a consistent power dissipation of 6 W/mm. These tests were performed at varying channel temperatures of 204 °C, 232 °C, and 260 °C, all maintained under the same voltage condition ($V_{DS} = 25$ V), over an approximate duration of 3000 hrs. [116]. However, a comprehensive analysis of activation energy and MTTF was notably absent from the study.

Under a consistent voltage condition of $V_{DS} = 30$ V, a high-temperature operating life (HTOL) test was executed for approximately 2000 h. This test encompassed three distinct channel temperatures: 210 °C, 225 °C, and 250 °C. The outcomes revealed a mean time to failure (MTTF) of 1.87×10^6 h at a temperature of 200 °C, along with activation energy (E_a) of 1.8 eV [117]. An accurate estimation of the channel temperature is of paramount importance for determining the precise mean time to failure (MTTF) values in GaN HEMTs. Employing a constant bias of $V_{DS} = 50$ V and a power dissipation rate of 4 W/mm, devices were subjected to stress testing at three distinct base temperatures: $T_b = 160$ °C, 175 °C, and 190 °C. However, the resulting MTTF values diverged based on the peak channel temperature (measured through Raman thermography) and the average temperature (measured via IR thermography). Specifically, two distinct MTTF values emerged: 10^9 h and 10^6 h [118].

Given the array of proposed stressors, degradation mechanisms, and associated degradation signatures, it is important to distinguish the precise stressors responsible for inducing

particular effects. All prior investigations were carried out on packaged GaN HEMT devices. Limited long-term reliability studies exist on GaN epitaxial wafers or on-wafer devices [119]. In the current study, we investigated the extraction of activation energy and MTTF values under two distinct stress conditions, denoted as high and low electric field stress in on-wafer devices.

Assessing the reliability of gallium nitride high-electron-mobility transistors (GaN HEMTs) under various electric field stress conditions is crucial for several reasons: Understanding how GaN HEMTs behave under different electric field stress conditions allows for the optimization of their performance and operational lifetime [120,121]. By identifying stress conditions that may lead to degradation, manufacturers can develop strategies to mitigate these effects and design devices that operate more reliably and durably. As we mentioned previously, GaN HEMTs are often used in high-power, high-frequency, and critical applications such as aerospace, defense, telecommunications, and power electronics. In these applications, device failures can have serious consequences, including system downtime, mission failures, or costly repairs. Assessing reliability helps prevent unexpected failures and ensures the uninterrupted operation of these systems [122,123]. In some applications, GaN HEMTs are used in safety-critical systems, where their failure could pose significant risks to human safety or the environment [124-129]. Reliability assessments under different stress conditions help identify potential failure modes and enable the implementation of safety measures and redundancies to mitigate these risks.

4.2 Condition of the Electric Field Stress

This methodology hinges on a crucial assumption: that failure mechanisms are thermally activated, and their relationship with temperature and failure rate follows the Arrhenius model. The accuracy of MTTF calculations depends on two key factors. First, the validity of the acceleration factor must be assured. Second, it assumes that the failure mechanisms observed during accelerated testing are representative of those encountered in normal operating conditions. The channel temperature (T_{ch}) of the device plays a pivotal role in determining the activation energy and acceleration factor. Temperature variations can exert a significant influence on device reliability. Hence, precise temperature measurements and control are paramount during accelerated testing. The accurate measurement and control of channel temperature are essential because temperature fluctuations have a direct impact on device reliability and shape the activation energy used in the model. Furthermore, this methodology presumes that failure

mechanisms are thermally activated and can be accelerated under stress conditions, thereby making the calculated MTTF values relevant to real-world device performance.

In this study, we delineate two distinct stress zones, each characterized by specific combinations of high current and low electric field, as well as low current and high electric field. To comprehensively investigate these zones, we carefully selected specific bias conditions. Specifically, we opted for two distinct bias zones: one at a low voltage (V_{DS} = 10 V) and another at a higher voltage (V_{DS} = 25 V), each accompanied by power dissipation rates of 2 W/mm and 1.25 W/mm, respectively. These selected bias parameters are concisely summarized in Table 1. Additionally, we conducted experiments at three varying base temperatures: T_b = 150 °C, 170 °C, and 190 °C. The determination of channel temperature for each bias condition is discussed in detail within the Results and Discussion section of this study.

Table 4.1 Selected test condition for determination of MTTF values.

Sample Quantity	Stress Voltage, V_{DS} (V)	Current, I_{DS} (mA/mm)	Power, P (W/mm)
5	10	200	2
5	25	50	1.25

Figure 4.1 represents output characteristics of GaN HEMTs device of gate length, L_g = 3 µm, source to drain distance, L_{sd} = 7 µm and gate width, W_g = 50 µm. The output characteristics show that at very high drain voltage (V_{DS} > 20 V) with an increase of gate voltage from V_{GS} = −1 V to 2 V leads to a decrease in output drain current (I_{DSS}) because of self-heating effects [130]. To gain insights into the influence of temperature and characteristics on stress performance.

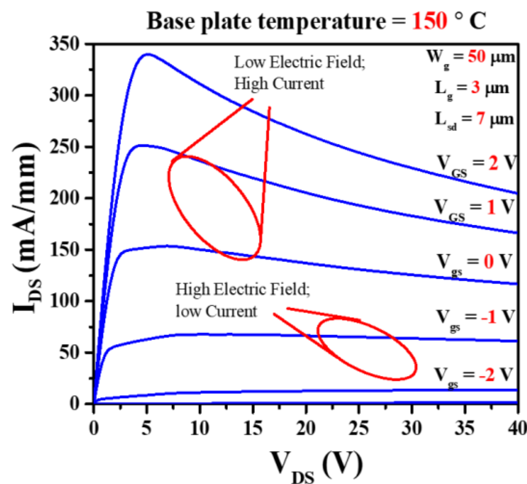


Figure 4.1. Output characteristics at base plate temperature 150 °C represent the stress zones of low electric field and high electric field.

4.3 Electric field and Channel temperature simulation

Figure 4.2 (a) and (b) represent the bias stress condition of low electric field (V_{DS} = 10 V and V_{GS} = 1.3 V set for 200 mA/mm, power dissipation, P = 2 W/mm) and high electric field (V_{DS} = 25 V and V_{GS} = −1 V set for 50 mA/mm, power dissipation, P = 1.25 W/mm). Under the low electric field stress condition, the device operates in a fully on-state condition, and a conspicuous self-heating effect is evident in the output characteristics (Figure 4.1). Consequently, this scenario closely resembles a high-power state condition. Conversely, during the high electric field stress condition, the device is in an off state, resulting in a minimal self-heating effect. This aligns with a high-voltage state in the off-state mode.

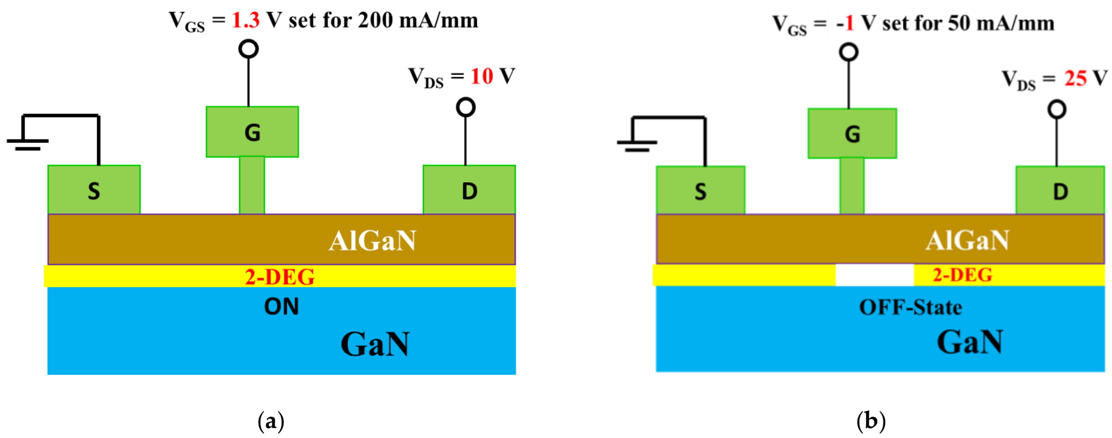


Figure 4.2 (a) Bias condition for low electric field and (b) high electric field region.

Figure 4.3 (a) shows the electric field simulation of stress voltage V_{DS} = 10 V and 25 V. A negligible electric field variation is evident inside the AlGaN barrier. Figure 5b illustrates the electric field simulation inside the GaN channel. At the gate edge to the drain side, the electric field increased 1.2 times higher at V_{DS} = 25 V than at V_{DS} = 10 V. As we mentioned above, stress condition V_{DS} = 25 V, V_{GS} = −1 V is in the off-state mode. Therefore, a negative voltage is applied to the gate of the GaN HEMT. This negative voltage creates a strong electric field that pushes electrons away from the channel region. The high electric field in the off state extends through the GaN material and depletes the 2DEG, preventing the flow of electrons in the channel. In the on-state condition (V_{DS} = 10 V, V_{GS} = 1.3 V), a less negative (or even positive) voltage is applied to the gate of the GaN HEMT. This reduces the electric field across the device. The reduced electric field allows the 2DEG to accumulate or populate near the interface between the GaN and AlGaN layers.

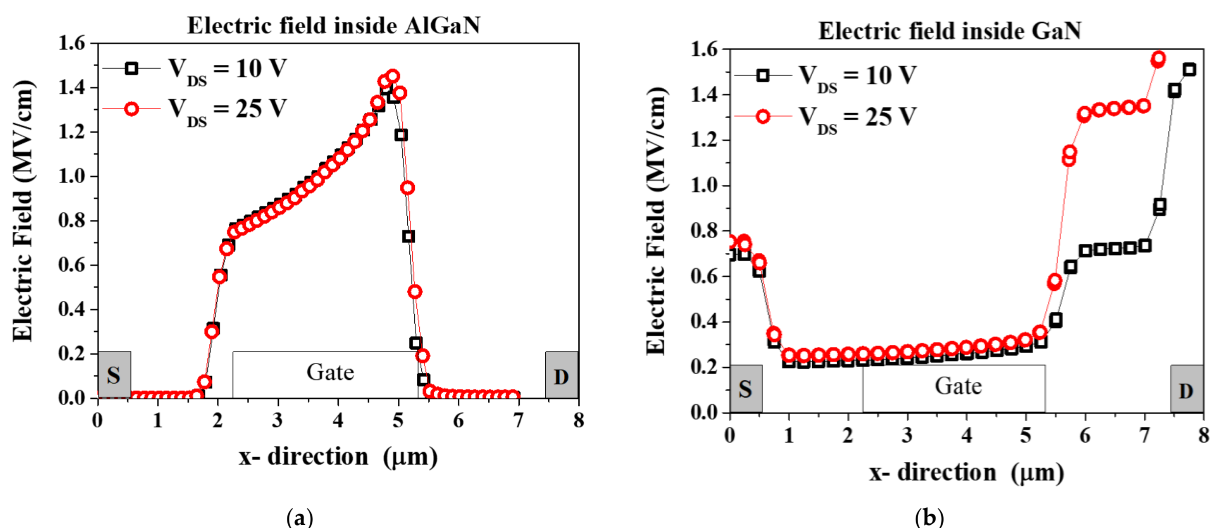


Figure 4.3. (a) Electric field simulation using Silvaco TCAD inside AlGaN barrier and (b) inside GaN channel.

The channel temperature measurement method, as discussed in Chapter 3, (Figure 3.8) is consistently applied in this context. Across a range of gate voltages, specifically from V_{GS} = 0 V to 2 V, the disparity in channel temperature (T_{ch}) remained negligible. For 2 W/mm and 1.25 W/mm power dissipation, channel temperature rise (T_{ch}) was approximately 60 °C and 38 °C, respectively, from the base plate temperature (T_b). Figure 7(a) depicts the simulation results for a device under V_{GS} = 0 V and V_{DS} = 10 V conditions while maintaining a base plate temperature of T_b = 300 K (27 °C). Notably, the highest channel temperature recorded was 327 K (54 °C) in close proximity to the gate edge.

Similarly, when the device was biased at V_{DS} = 25 V with the same gate voltage, V_{GS} = 0 V, the corresponding channel temperature escalated to 360 K (87 °C), as illustrated in Figure 7b. This change corresponds to an approximate temperature increase of 33 °C. Consequently, the temperature variation within the channel is contingent upon the stress voltage conditions. To determine the changes in channel temperature (T_{ch}) resulting from fluctuations in drain currents, we conducted experiments to observe the behavior of drain currents under different temperature conditions. Our findings indicated a consistent linear decrease in drain current across various temperature settings [131]. Additionally, we computed power levels ($I_{DS} \times V_{DS}$) from the output characteristics of the device. Subsequently, we normalized the drain current data relative to different temperatures and power levels. These normalized values were used to construct graphs in Figure 3.13 (measurement data), representing the relationship between channel temperatures and power levels. Notably, this exhibits a remarkable congruence between the TCAD simulation outcomes and our measurement data.

4.4 Low Electric Field with High Current Stress Experiment

Figure 4.4 (a) presents the transfer characteristics (characterization at V_{DS} = 10 V) at low electric field stress condition at V_{DS} = 10 V and output current level maintained to I_{DS} = 200 mA/mm for power dissipation of P = 2 W/mm. At a constant base plate temperature of T_b = 150 °C the channel temperature was estimated as T_{ch} = 215 °C. After 84 h of stress, I_{DS} and g_m dropped around 30 mA/mm and 18 mS/mm, respectively. At the same time, gate leakage current I_G (defined at V_{GS} = −10V, V_{DS} = 10 V) increased from 3.3×10^{-4} to 0.034 mA/mm, as shown in Figure 4.4 (b). The threshold voltage negatively shifted around ΔV_T = −0.16 V. After 175 h of stress, I_{DS} and g_m decreased more around 38 mA/mm and 31 mS/mm, respectively, from the initial value (Figure 4.4). At the same point, the leakage current increased from the initial value of 3.3×10^{-4} to 0.051 mA/mm, and the threshold voltage shift was around ΔV_T = −0.31 V from the initial value.

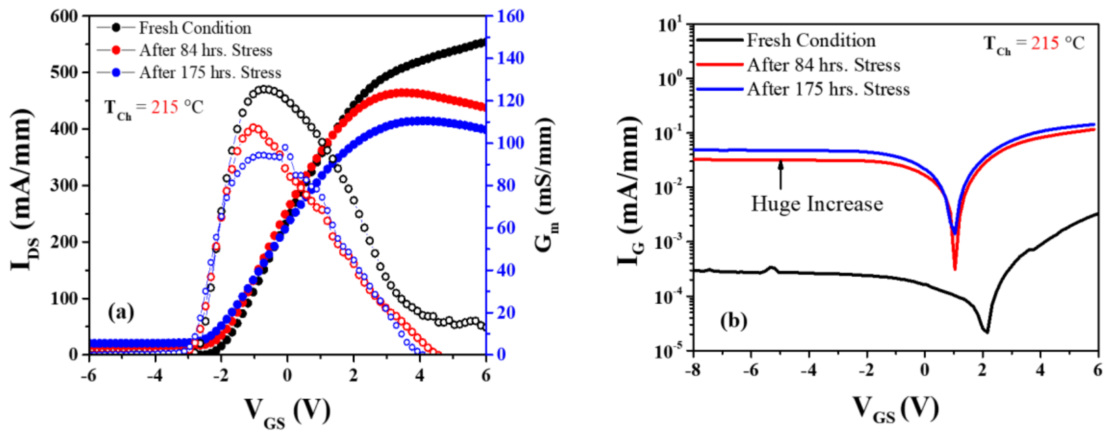


Figure 4.4 (a) Transfer characteristics after and before stress voltage V_{DS} = 10 V; (b) Schottky characteristics depict gate leakage current after stress at the channel temperature, T_{ch} = 215 °C.

Figure 4.5 (a) shows the output characteristics before and after stress of 84 h and 175 h. On-resistance (Ron) increased around ΔR_{ON} = 20 Ω·mm at V_{GS} = 0 V after 84 h of stress, and no change was observed until 175 h. The failure time is defined at I_{DSS} degradation up to 15%.

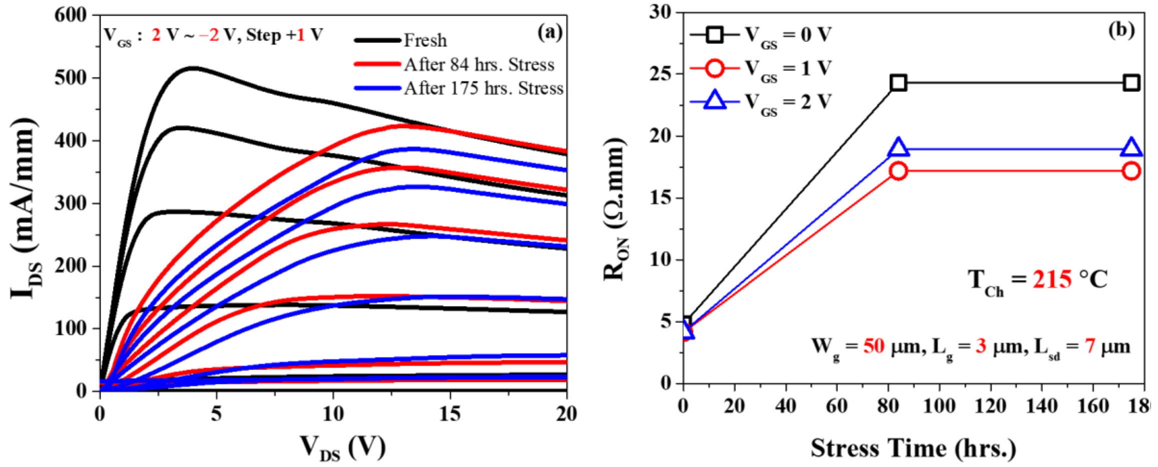


Figure 4.5. (a) Output characteristics after and before the stress of V_{DS} = 10 V; (b) on-resistance characteristics after and before stress voltage at V_{DS} = 10 V.

All the degradation in the other two base plate temperatures (T_b = 170 °C and 190 °C) are depicted in Table 4.2.

Table 4.2. Lifetime calculation at different base plate temperatures for low electric field stress.

Base Plate Temperature (T_b) °C	Corresponding Channel Temperature (T_{ch}) °C	Condition	Lifetime (h) (15% Degradation)
150	215	V_{DS} = 10 V,	175
170	230	I_D = 200 mA/mm	147
190	240	P = 2 W/mm	120

4.5 High Electric Field with Low Current Stress Experiment

Figure 4.6 (a) shows the transfer characteristics at high electric field stress V_{DS} = 25 V, I_{DS} = 50 mA/mm, and the power dissipation set at 1.25 W/mm. After 36 h of stress, there seemed a slight increase in the output current from 387 mA/mm to 401 mA/mm at the base plate temperature of T_b = 150 °C. The maximum transconductance (g_{max}) also showed negligible change. But at the same time, the leakage current I_G increased from 9.12 × 10^{-5} mA/mm to 3.86 mA/mm, whereas no shift was observed in the threshold voltage (ΔV_T), as shown in Figure 4.6 (b). After 62 h of stress, the output current (I_{DS}) decreased around 84 mA/mm from its initial value, and g_m also decreased from 337 mS/mm to 313 mS/mm (almost 24 mS/mm). However, no change was observed in the leakage current. Table 3 illustrates the degradation observed at the other two base plate temperatures, namely T_b = 170 °C and 190 °C.

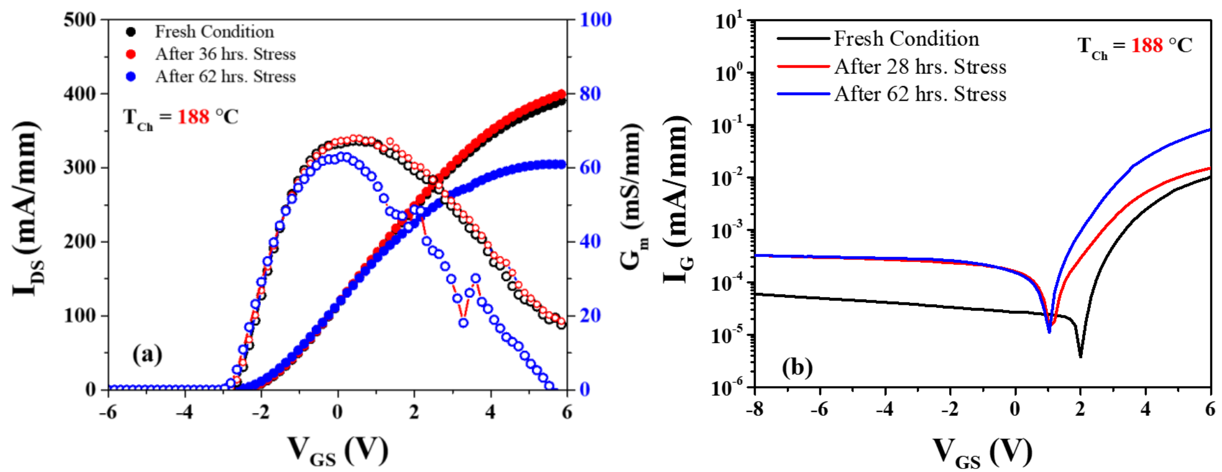


Figure 4.6. (a) Transfer characteristics after and before stress voltage V_{DS} = 25 V; (b) Schottky characteristics depict gate leakage current after stress at the channel temperature 188 °C.

Figure 4.7 (a) illustrates the output characteristics prior to and following stress periods of 36 h and 62 h. After 32 h of stress, I_{DSS} exhibited an increase, but this trend reversed after 62 h of stress. Notably, the on-state resistance (R_{on}) demonstrated an increase of approximately ΔR_{on} = 60 Ω·mm at V_{GS} = 0 V after 32 h of stress, with no noticeable alteration observed until the 62 h stress point. The degradation observed at the other two base plate temperatures, i.e., T_b = 208 °C and 228 °C, is depicted in Table 4.3.

Table 4.3. Lifetime calculation at different base plate temperatures for High electric field stress.

Base Plate Temperature (T_b) °C	Corresponding Channel Temperature (T_{ch}) °C	Condition	Lifetime (h) (15% Degradation)
150	188	V_{DS} = 25 V, I_D = 50 mA/mm P = 1.25 W/mm	62
170	208		36
190	228		15

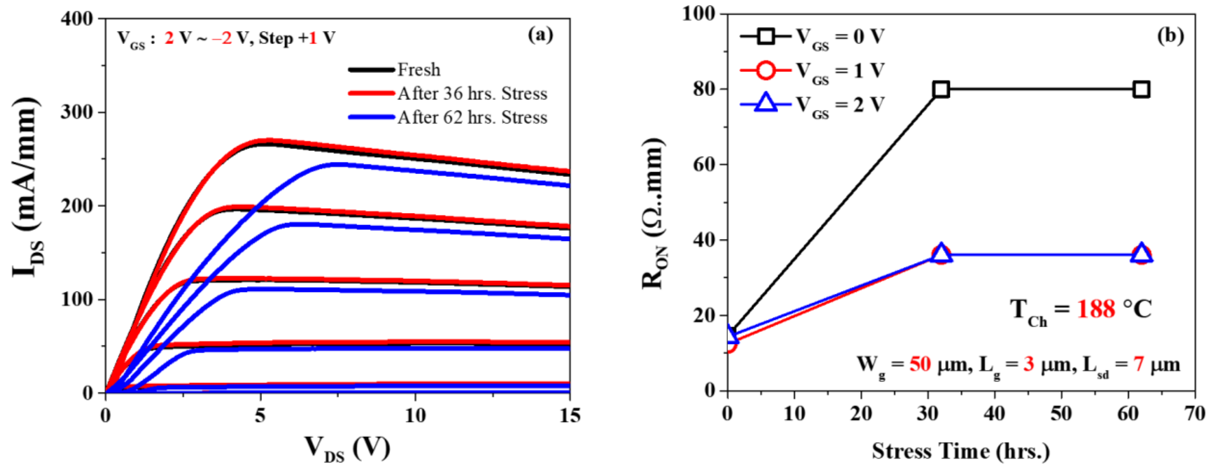


Figure 4.7. (a) Output characteristics before and after the stress of V_{DS} = 25 V; (b) on-resistance characteristics before and after stress voltage at V_{DS} = 25 V.

4.6 Mean time to failure analysis

Figure 4.8 (a) demonstrates the degradation of I_{dss} (which is defined at V_{DS} = 5 V and V_{GS} = 2 V) in three different channel temperatures calculated for the V_{DS} = 10 V bias condition. No abrupt degradation behavior of I_{dss} was observed in high temperatures. However, under high-stress voltage conditions (V_{DS} = 25 V), the device's stability was compromised, lasting no more than 15 h at T_{ch} = 228 °C, as depicted in Figure 4.8 (b).

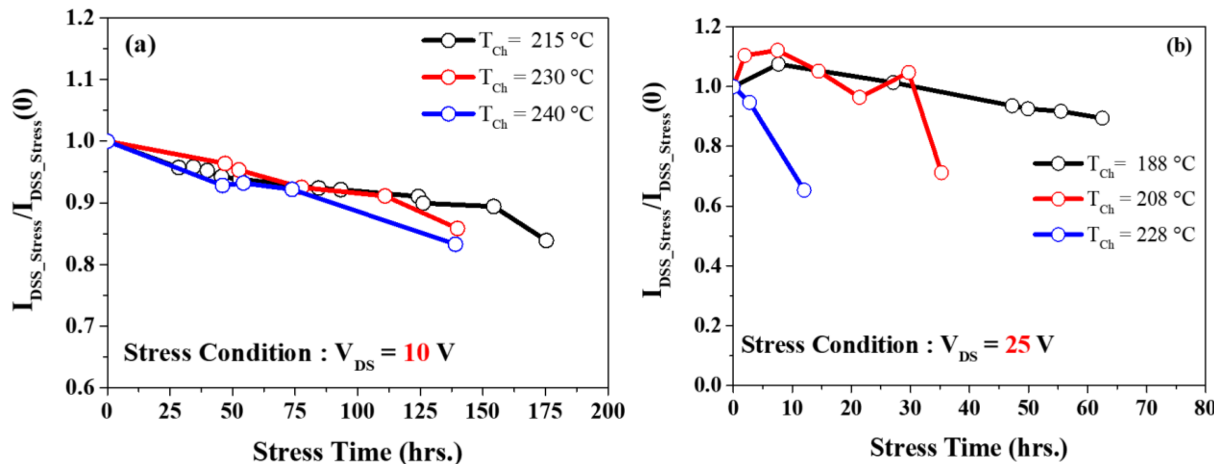


Figure 4.8. (a) **I_{DSS} degradation at low electric field stress voltage V_{DS} = 10 V and (b) high electric stress voltage V_{DS} = 25 V.**

Figure 4.9 illustrates the *MTTF* values calculated for three different channel temperatures under specific voltage stress conditions. To calculate the activation energy, the well- known Arrhenius equation of mean time to failure (*MTTF*) can be expressed as follows :

$$MTTF = e^{-\left(\frac{E_a}{KT}\right)}$$

$$\ln[MTTF] = -\frac{E_a}{kT} \quad (4.1)$$

Here, $MTTF$ = mean time to failure; k = Boltzmann constant, 8.6173×10^{-5} eV K^{-1}; and E_a = activation energy (eV). From the slope of Equation (3), activation energy (E_a) can be calculated.

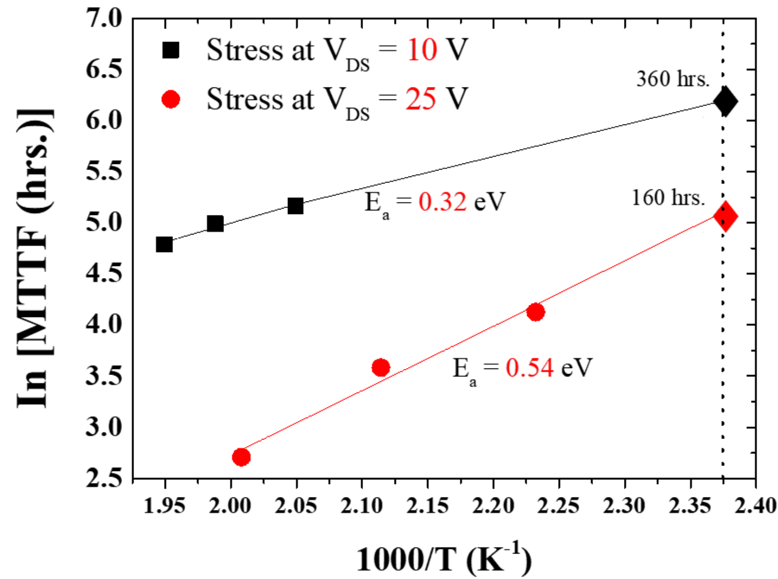


Figure 4.9. Mean time to failure (*MTTF*) analysis of two different electric field conditions.

Under the low electric field stress condition (V_{DS} = 10 V), the calculated activation energy was E_a = 0.32 eV, yielding an extrapolated lifetime MTTF = 360 h. Conversely, under the high electric field stress condition (V_{DS} = 25 V), the estimated activation energy was E_a = 0.54 eV, resulting in MTTF = 160 h. The possible degradation or failure at low electric field and high current stress is related to the diffusion process (E_a = 0.32 eV). This diffusion can lead to the formation of conductive paths or short circuits within the device, increasing leakage current and reducing the breakdown voltage. For the high electric field and low current stress, this degradation is related to the hot-electron effect or electron trapping (E_a = 0.54 eV) [132]. The obtained mean time to failure (MTTF) values for GaN high-electron-mobility transistors (HEMTs) are significant indicators of device reliability and can provide insights into their performance under different electric field stress conditions. In general, MTTF represents the expected time for a device to fail under specified conditions. It is a critical parameter for assessing device reliability. We calculated MTTF values for on-wafer GaN HEMTs under both low (V_{DS}

= 10 V) and high (V_{DS} = 25 V) electric field stress conditions. These values indicate how long, on average, the devices can be expected to operate before a significant number of them fail. The lower MTTF under high electric field stress (160 h) suggests that the devices are more prone to failure when subjected to higher voltage stress, which is consistent with accelerated aging in high-stress conditions.

Our MTTF values were validated only for on-wafer/bare-wafer devices. The MTTF for on-wafer devices typically represents the reliability of the semiconductor material itself, without considering packaging and external factors. On the other hand, the MTTF for packaged devices takes into account not only the intrinsic reliability of the semiconductor material but also the effects of packaging, assembly, and the device's operational environment. Packaged devices typically have a longer MTTF than bare wafers because their packaging contributes to their robustness and resilience. In summary, comparing the MTTF of a bare-wafer device with a packaged device is not a straightforward apples-to-apples comparison.

4.8 Summary

The presentation of MTTF data for on-wafer devices was contingent upon specific electric field conditions. The accurate determination of channel temperature assumes a critical role in the precise estimation of MTTF values. Furthermore, degradation parameters exhibited variations based on the specific stress voltage or electric field conditions. Moreover, when calculating MTTF for on-wafer devices, distinct electric field conditions yielded different values. These intricate details merit thorough consideration as they hold the potential to significantly enhance the long-term reliability of AlGaN/GaN HEMTs.

Chapter 5

Degradation Physics

In the previous chapter, we delved into various stress methodologies and their influence on device performance, exploring how degradation parameters respond to diverse voltage and temperature conditions. We also emphasized the significance of accurately determining channel temperature in the context of HTOL testing and underscored the importance of considering combined acceleration factors. It became evident that device degradation is not solely temperature-dependent but also influenced by the electric field in AlGaN/GaN HEMTs. In this chapter, we delve deeper into the degradation mechanisms responsible for device performance and provide a comprehensive understanding of the underlying physics.

5.1 Investigated Devices

Throughout this thesis, numerous transistors underwent testing under direct current (DC) conditions. In this chapter, we present the findings related to three distinct devices of AlGaN/GaN HEMTs that were subjected to similar stress conditions. Additionally, these high-electron-mobility transistors (HEMTs) originated from wafers processed around the same period, enabling a comparative analysis of various technologies. Minimum 5 devices are necessary to performed HTOL test at one temperature for each type of HEMTs. A significant quantity of devices is essential when conducting tests at various temperatures to establish an acceleration model. The description of three distinct HEMTs samples is summarized as follows:

- **Sample A**

  Sample A HEMTs epi structure were synthesized utilizing a low-pressure metal–organic chemical vapor deposition (MOCVD) technique on 3-inch SiC wafers measuring 398 μm in thickness. The epi-structures consist of an 8 nm $Al_{0.45}Ga_{0.55}N$ barrier layer, a 420 nm channel layer, and a 270 nm GaN buffer in the SiC shown in Figure 5.1 (a). The

reliability test was performed on specific device condition, W_g = 50 µm, L_g = 3 µm, and L_{sd} = 7 µm. All these devices underwent characterization, involving the plotting of their output characteristics, transfer characteristics, and their I-V gate characteristics. The Hall mobility measured at 1591.8 cm^2/Vs, 2DEG density (n_s) found to be 0.954×10^{13} cm^{-2} and the sheet resistance was measured at 411.3 ohm/sq.

- **Sample B**

  Sample B HEMTs epi structure was grown via the low-pressure metal-organic chemical vapor deposition (MOCVD) technique on 3-inch SiC wafers. The epi-structures consist of an 8 nm $Al_{0.45}Ga_{0.55}N$ barrier layer, a 40 nm channel layer, a 400 nm AlGaN Back barrier (BB), and a 270 nm GaN buffer in the SiC depicted in Figure 5.1 (b). The significant difference between structure A and B is the inclusion of 400 nm AlGaN BB and low channel thickness 40 nm. In sample B, hall mobility value found 1367.4 cm^2/Vs, 2DEG density (n_s) calculated at 0.823×10^{13} cm^{-2} and the sheet resistance value depicted 555.4 ohm/sq.

- **Sample C**

  Sample C HEMTs epitaxial layer structures were developed through MOCVD technique on 3-inch SiC wafers. This epitaxial configuration comprised an $Al_{0.25}Ga_{0.75}N$ barrier layer (20 nm), a Ga-polarity GaN channel layer (150 nm), and a high-resistance GaN layer (2.4 µm) positioned atop the sapphire substrate. The schematic can be observed in Figure 4.1(c). The high resistance GaN layer doped with carbon (C) with density of 5×10^{18} cm^{-3}. Compared to samples A and B, sample C exhibits an almost typical structure, but the increased doping in the buffer layer enhances its long-term reliability. We will delve into this in the subsequent discussion and experiments. In sample C, hall mobility value found 2000-2200 cm^2/Vs, 2DEG density (n_s) calculated at 9×10^{12} cm^{-2} and the sheet resistance value depicted 600 ohm/sq.

Table 5.1 Summary of technological data of the transistor sample.

Sample Type	Epitaxy	Al(%)	Doping	Gate	Ohmic
A	AlGaN	45%	n.i.d	Ni/Au	Ti/Al/Ni/Au
	GaN	-	n.i.d		
B	AlGaN	45%	n.i.d		
	GaN	-	n.i.d		
	AlGaN BB	-	n.i.d		
C	AlGaN	25%	n.i.d		
	GaN	-	n.i.d		
	High resistance GaN	-	Carbon (C)		

5.2 Measurement Setup

The measurement system includes MS Micro-tech probe station (Model: MS TECH 5500) with temperature controlled (Model: Temptronic TP03000) heating plate, ensuring precise temperature control during the I–V (current–voltage) characteristic measurements before and after stress. The measurements can be conducted in two modes such as Monitoring mode and Read-out measurement. During the stress, the bias point parameters are continuously monitored (I_{DS}, V_{DS}, I_{GS}, and V_{GS}), enabling us to track the transistor's behavior over time. After each stress test, the device is measured to evaluate the degradation of its electrical parameters without cooling the temperature. Besides the parameters previously defined, the device is characterized by plotting its characteristics curves: Output I-V characteristics I_{DS} *vs.* V_{DS} as a function of V_{GS} for n values of V_{GS} ($0< n < 20$) and transfer characteristics I_{DS} *vs.* V_{GS} as a function of V_{DS} for n values of V_{DS} ($0< n < 10$). The failure criteria of the device are set to 15% degradation of the I_{DSS}. The schematic of the test methodology is given in Figure 5.1 :

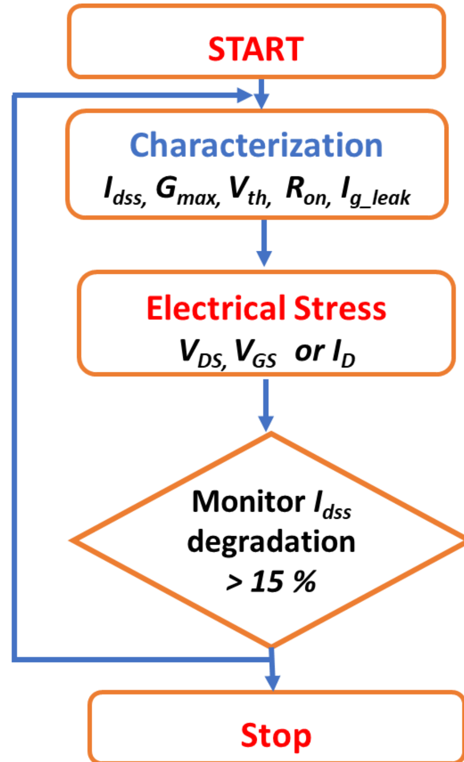


Figure 5.1: Characterization and Methodology of the HTOL Stress Experiment

5.3 Basic Parameter degradation and comparison among the HEMTs

The test condition was set to V_{DS} = 15 V and maintained constant power dissipation, P_D = 2 W/mm for all the HEMTs sample. The test was conducted in three base plate temperature, T_b = 175 °C, 190 °C & 210 °C and for these base plate temperatures, the corresponding channel temperature is estimated T_{ch} = 210 °C, 225 °C & 245 °C respectively for sample A and B. In sample C, the channel temperatures are little bit higher, and it is estimated as T_{ch} = 245 °C, 260 °C & 290 °C for the same base plate temperatures. For systematic analysis, at least 5 devices were stressed for each operating condition. Figure 5.2 shows the transfer characteristics of all HEMTs sample before and after stress condition. The stress stopped after 15% degradation of I_{Dmax}. Within this time duration, sample A, sample B and sample C sustained around 40 hrs., 47 hrs., and 132 hrs. respectively. The degradation of the drain current (I_{DS}) and maximum transconductance (g_{max}) are depicted in table 5.2.

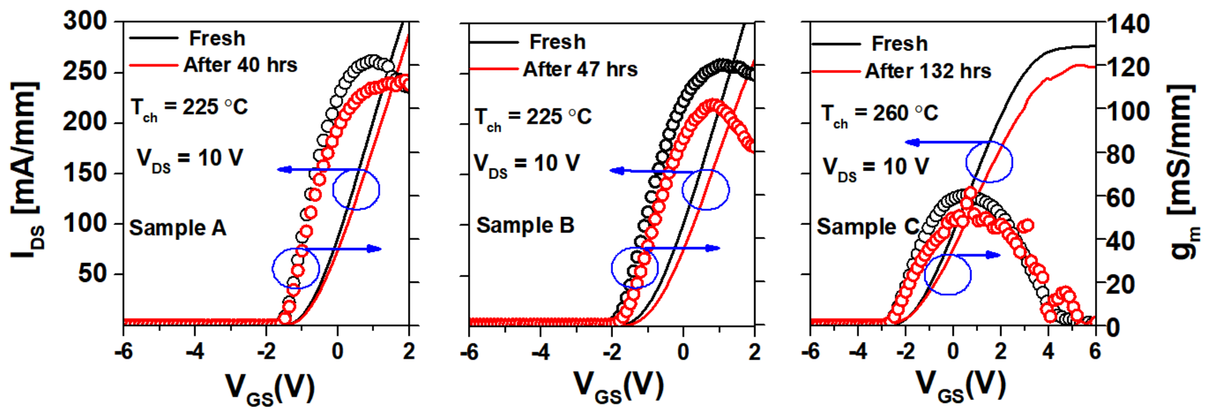


Figure 5.2: Transfer characteristics of the samples before and after stress condition.

Table 5.2 The degradation of maximum drain current (I_{Dmax}), maximum transconductance (g_{max}) and the threshold voltage (ΔV_T) shift after stress.

Test Samples	**I_{Dmax} (mA/mm) @ V_{GS} = 1 V**		**g_{max}(mS/mm)**		**ΔV_T (V)**	
	Before	After	Before	After	Before	After
Sample A	202	171	262	234	-0.7	-0.75
Sample B	243	190	120	100	-1.0	-1.1
Sample C	150	125	60	50	-1.0	-1.20

The output characteristics of the devices are shown in Figure 5.3. The I_{DS}- V_{DS} characteristics plotted for the all HEMTs at V_{GS} = 1 V per step. The figure depicted that the highest degradation of the drain current (I_{DS}) observed at sample B. Compared to sample A and B, sample C exhibit low drain current degradation at high drain bias.

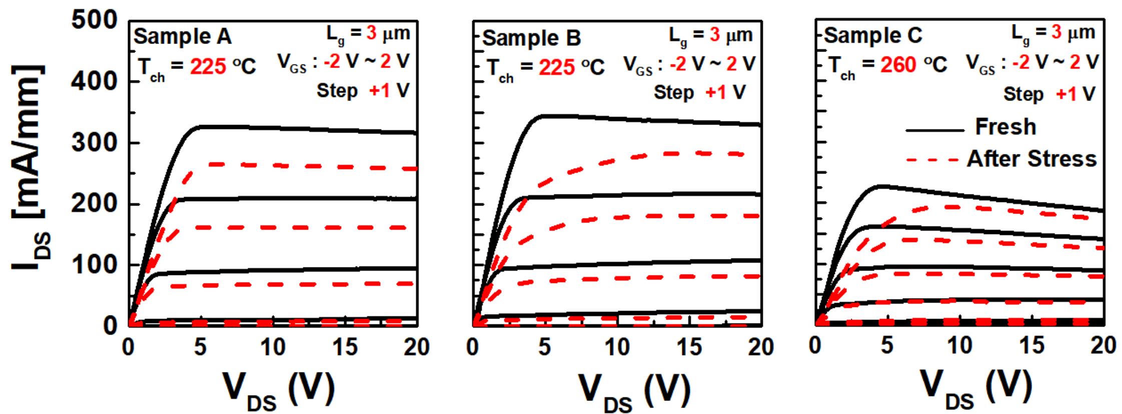


Figure 5.3: I_{DS} degradation (15%) after stress at V_{DS} = 15V and constant power dissipation P_w = 2 watt/mm in all samples at the same base plate temperature (T_b = 190 °C).

The comparison of the I_{DS} degradation of all samples are shown in Figure 5.4. The I_{DSS} degradation is defined at V_{DS} = 5 V; V_{GS} = 1 V. At all base plate temperatures, T_b = 175 °C, 190 °C & 210 °C, I_{DSS} degradation plotted against the stress time (hrs.). In sample A, at low temperature, T_b = 175 °C, the device sustains around 55 hrs. and at high temperature, T_b = 210 °C, there observed sharp degradation and more than 50% of I_{DSS} degradation occurred within 25 hrs. of stress. In sample B, abrupt or sudden degradation is observed at T_b = 190 °C, the device burnt out after 40 hrs. of stress. At low temperature, T_b = 175 °C., it seems quite stable and sustains up to 60 hrs. Compared to sample A and B, sample C shows quite stable and the longest lifetime. In sample C, the devices sustain around 300 hrs. of stress and up to 100 hrs. of stress, the device showed 60 % I_{DSS} degradation and remain stable until 300 hrs. at low temperature, T_b = 175 °C. At high temperature, T_b = 210 °C, this device shows sudden degradation after reaching 100 hrs. of stress condition.

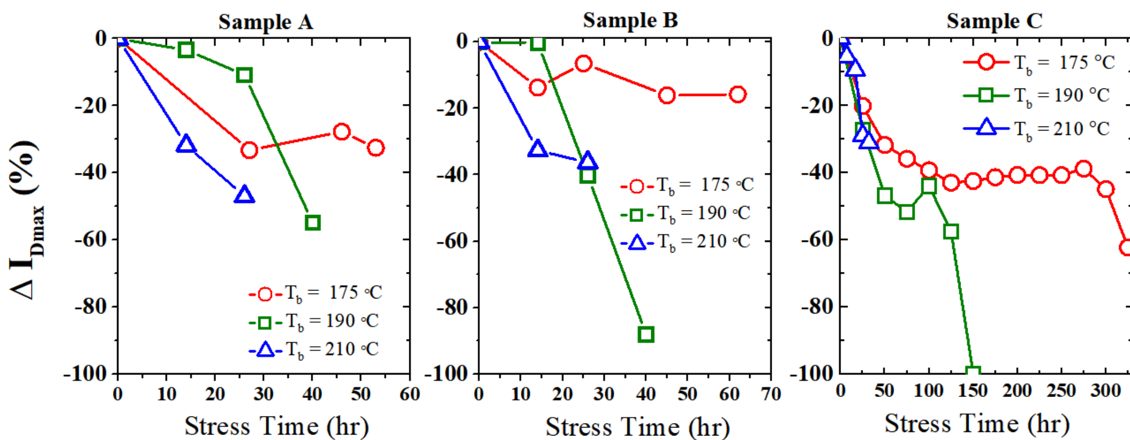


Figure 5.4 Comparison of the I_{Dmax} degradation

The comparison of the threshold voltage shift (ΔV_T) among the samples is plotted in Figure 5.5. At low temperature, T_b = 175 °C, sample A shows no threshold voltage shift up to 30 hrs. of stress and after that it goes to positive direction and shift is very high around 1.6 V. In sample B, the trend of ΔV_T shift goes negative direction but after 25 hrs. of stress it shows shifting in little positive direction. Whereas, in sample C, the ΔV_T shift goes negative direction throughout the stress time. At medium temperature, T_b = 190 °C, sample A shows no ΔV_T shift bu in sample B, after 15 hrs. stress, ΔV_T goes to positive direction (-1.5 V) and then falls down to -0.8 V (negative direction), and after that it goes again positive direction. In sample C, ΔV_T goes to negative direction until 75 hrs. of stress and then it goes positive direction, back to its original position after 90 hrs. of stress. After that it goes again to the negative direction and the highest negative shifting observed around -0.2 V. At high temperature, T_b = 210 °C, all the samples A, B and C shows negative ΔV_T shift.

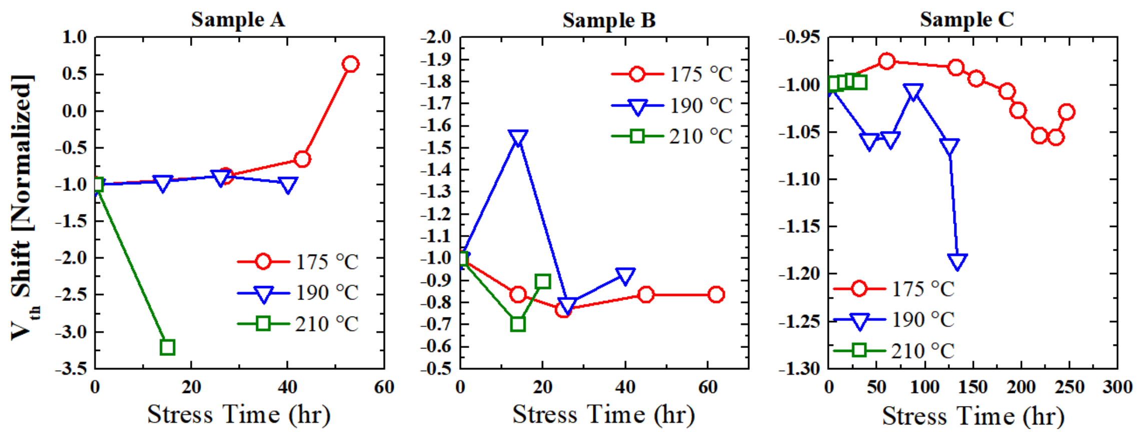


Figure 5.5 Comparison of the threshold voltage shift (ΔV_T).

In Figure 5.6, there depicted g_{max} degradation comparisons among three samples. First of all, at low temperature, T_b = 175 °C, g_{max} degraded around 25 % after 25 hrs. of stress observed at sample A. Compared to sample A, sample B remains stable and there observed 15% degradation after 60 hrs. of stress. In sample C, the g_{max} degradation looks pretty stable and it found around 40% degradation after 250 hrs. of stress. At medium temperature, T_b = 190 °C, sample A shows quit stable and gradual fall of g_{max} up to 40 hrs. of stress. In sample B, sudden g_{max} degradation observed after 25 hrs. of stress. Compared to sample A and B, sample C shows steady g_{max} degradation and around 20% degradation observed after 130 hrs. At high temperature, T_b = 210 °C, the value of g_{max} in sample A falls abruptly only after 15 hrs. of stress. Compared to sample A, sample B shows 15 % degradation after 20 hrs. of stress. In sample C, the trend of the g_{max} degradation seems stable up to 115 hrs. of stress and then falls at 15% after 150 hrs. of stress.

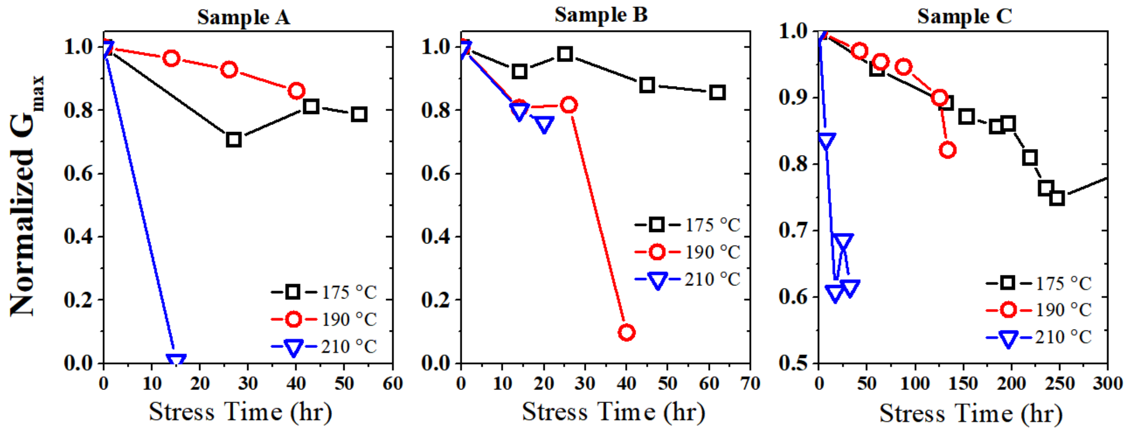


Figure 5.6 Comparison of the maximum transconductance (g_{max}) degradation among the samples.

Figure 5.7 shows the leakage current comparison of three samples after stress. At low temperature, T_b = 175 °C, there observed all most negligible leakage current (I_{g_leak}) increase in sample A. Compared to sample A and C, sample B shows the highest leakage current increase which is 2 times higher than its original value. And sample C also shows low leakage current increase throughout the stress time. At medium temperature, T_b = 190 °C, sample A shows low leakage current increase but in sample B shows decrease of the leakage current.

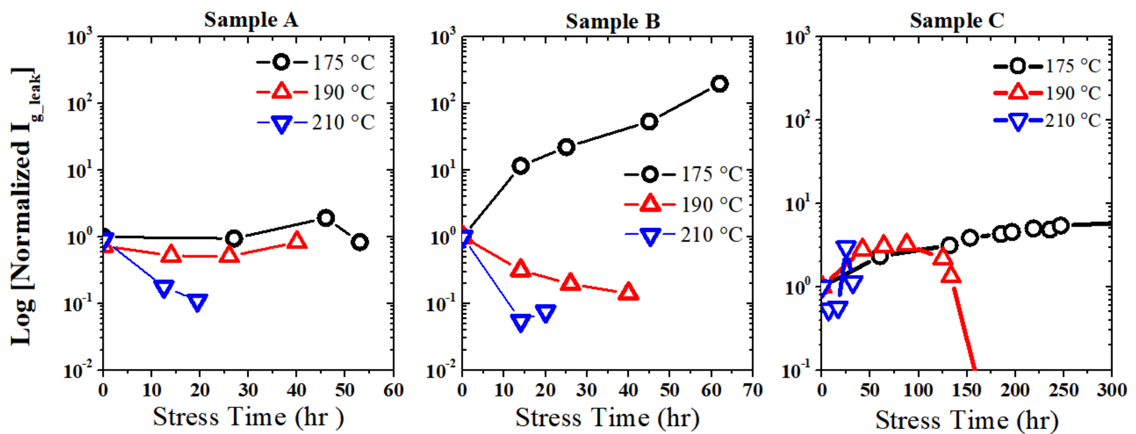


Figure 5.7 Comparison of the maximum transconductance (g_{max}) degradation among the samples.

In sample C, there is observed little bit increment of leakage current up to 100 hrs. of stress and then leakage current falls. At high temperature, T_b = 210 °C, sample A and B show decrease of the leakage current and in sample C values are quite stable nor increase either decrease.

In Figure 5.8, the comparison of On-resistance (R_{on}) is shown among the samples. At low temperature, T_b = 175 °C, R_{on} is not so much increase in sample A. Compared to sample A, sample B shows pretty good increment from 30 Ω.mm to 45 Ω.mm. In sample C, this exhibit very stable results and it is increased gradually from 20 Ω.mm to 50 Ω.mm around 300 hrs. of stress. At medium temperature, T_b = 190 °C, sample A shows little increase of R_{on} around 50 % and sample B also shows 40 % of increment. But in sample C, the increment of R_{on} is very less which around 10 %. At high temperature, T_b = 210 °C, sample A shows the worst condition where the value of R_{on} increased around 500%. In sample B it also 300 %, where as in sample C, the increment of R_{on} is only 15%. Among all three sample, sample C exhibit very stable condition.

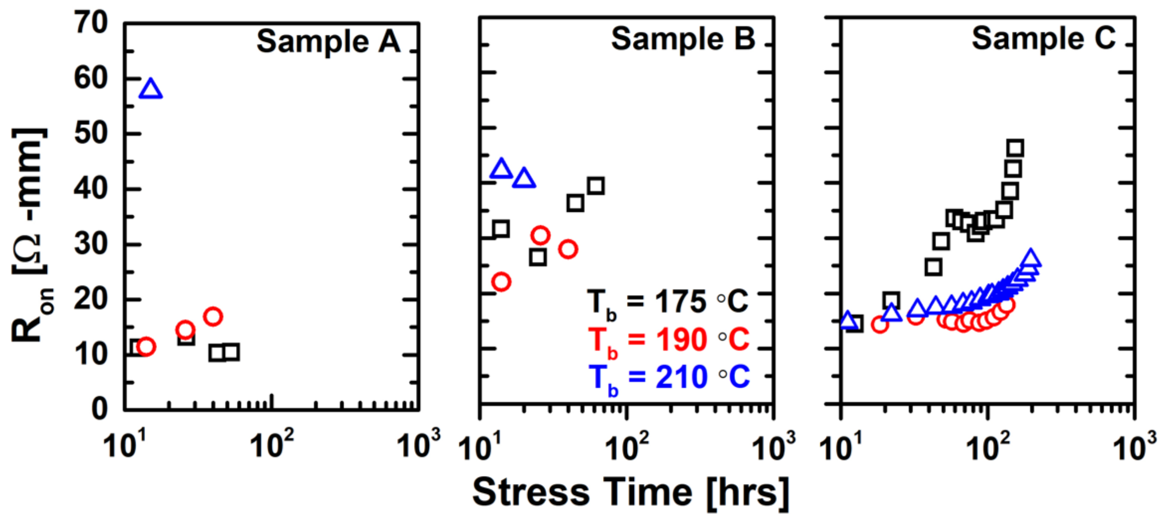


Figure 5.8 Comparison of the On-resistance (R_{on}) degradation among the samples.

5.4 Discussion of Electrical Degradation

To investigate the electrical degradation physics, we plotted the ($Ig \times Id$) product against V_{GS} in all three samples after each stress interval. Figure 5.9 shows the graph of sample A, B and C. Before discussing the details of the results, we delve into the importance of ($Ig \times Id$) product. The intensity of the EL (electroluminescence) signal generated by Bremsstrahlung [133, 134] is directly proportional to the density/energy of hot electrons in the channel. Bisi et al. reported that EL intensity is proportional to the ($Ig \times Id$) product which is a strong signature of hot-carrier and impact ionization mechanisms [135]. In the case of GaAs transistors, previous studies [136-138] have demonstrated that when hot electrons are present, the intensity of the electroluminescence (EL) signal is directly proportional to the product of gate and drain current.

This observation is made under the assumption that the rate of recombination of electrons and holes (EL signal) is proportional to both the electron density (I_D) and the hole density (I_G), which are generated by impact ionization.

Another study demonstrated that during on-state stress, it is observed that devices experience a substantial reduction in drain current and a decrease in the electroluminescence (EL) signal [139]. The degradation rate is closely linked to the intensity of the electroluminescence (EL) signal measured during stress on the devices. This signal is associated with the concentration of hot electrons in the channel. In our discussion, we related these two phenomena for explaining the degradation physics of the devices.

In sample A, the product ($Ig \times Id$) is decreasing while increasing the stress. At fresh condition, the value of the product found to be 60 nA^2 at V_{GS} = 2 V. And after 14 hrs. of stress, the value decreased to 55 nA^2 and more stress after 40 hrs., it is found around 50 nA^2. In sample B, the value of the product in fresh condition is 30 nA^2. After 25 hrs. of stress, this value going down to 8 nA^2 at V_{GS} = 2 V. The value of the product is continuously going down after stress. In sample C, the value of ($Ig \times Id$) in fresh condition is found around 200 nA^2 at V_{GS} = -1 V . After 25 hrs. of stress, the value is little bit decrease to 180 nA^2. But after 150 hrs. of stress, the value of ($Ig \times Id$) is increasing and it is found to 300 nA^2. And after 250 hrs. of stress, the value increased around 600 nA^2 and continuously increased up to 700 nA^2 until the device burnt out.

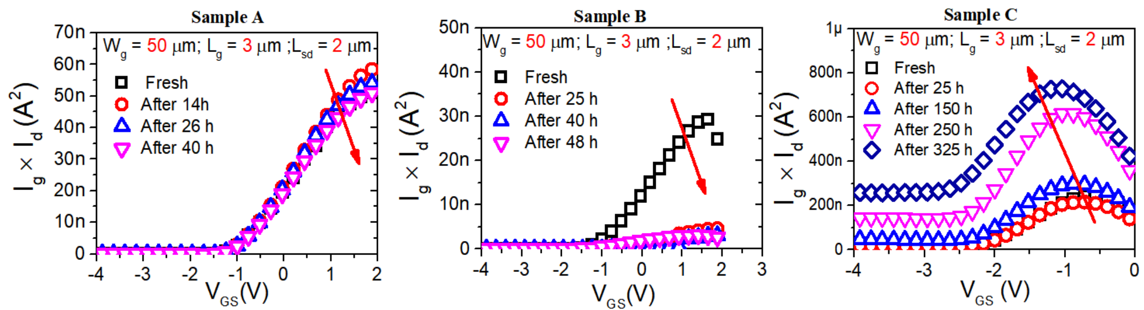


Figure 5.9: Comparison of *Ig* × *Id* in all samples against V_{GS}.

Figure 5.10 shows the relation of I_{DSS} degradation and $Ig \times Id$ product among the samples. In sample A, the relation of I_{DSS} degradation and $Ig \times Id$ product is shown linear. In sample B, the relationship is almost linear through the stress time. This behavior showing the degradation of I_{DSS} is proportional to the EL intensity and it supports the reference results Meneghini et al. [139]. That is clear evidence of hot electron related degradation in the devices sample A and sample B.

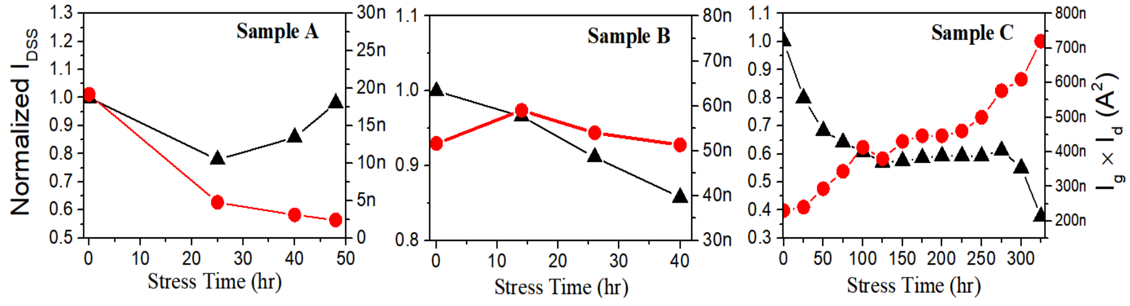


Figure 5.10: Relation between I_{DSS} degradation and $Ig \times Id$ product

But in sample C, the relationship seems reciprocal which supports the impact ionization related mechanisms reported by Bisi et.al. The strong correlation between $Ig \times Id$ product [electroluminescence (EL) intensity] and non-monotonic gate leakage suggests that hot electrons can substantially affect the electrical characteristics of the devices. Our explanation centers on impact ionization: when electrons reach the drain-side edge of the gate (where the electric field is at its maximum), they accumulate sufficient energy to initiate impact ionization, leading to the generation of electron-hole pairs. This phenomenon plays a crucial role in device degradation. The difference between the previous hypothesis and our result is that this is first time we have observed impact ionization at AlGaN/GaN HEMTs in long-term reliability assessment. From the report of Brar et al.,[140] impact ionization behaves strongly in high performance AlGaN/GaN HEMTs in low temperature. While increasing the temperature, impact ionization phenomena (related to kink effect) faded away.

We investigated completely different phenomenon which found in AlGaN/GaN HEMTs in high temperature and under electrical stress test. To prove impact ionization mechanism, we investigate the relationship of failure time with $|I_G|/I_D$ of all the devices. A common MOSFET acceleration law relates degradation and failure time to the impact ionization ratio, which is proportional to the ratio $|I_G|/I_D$ in Schottky-gate FETs [141]

$$t_F = \frac{F}{I_D(\frac{|I_G|}{I_D})m} \tag{5.1}$$

Figure 5.11 depicted the results of failure time with $|I_G|/I_D$ for all the samples. The fit of our data given by the above equation shown in Figure 5.12 (F = 5 h mA/mm, m = 1). In the case of sample C matched well with the fit, pointing out to the the importance of impact ionization in the device degradation.

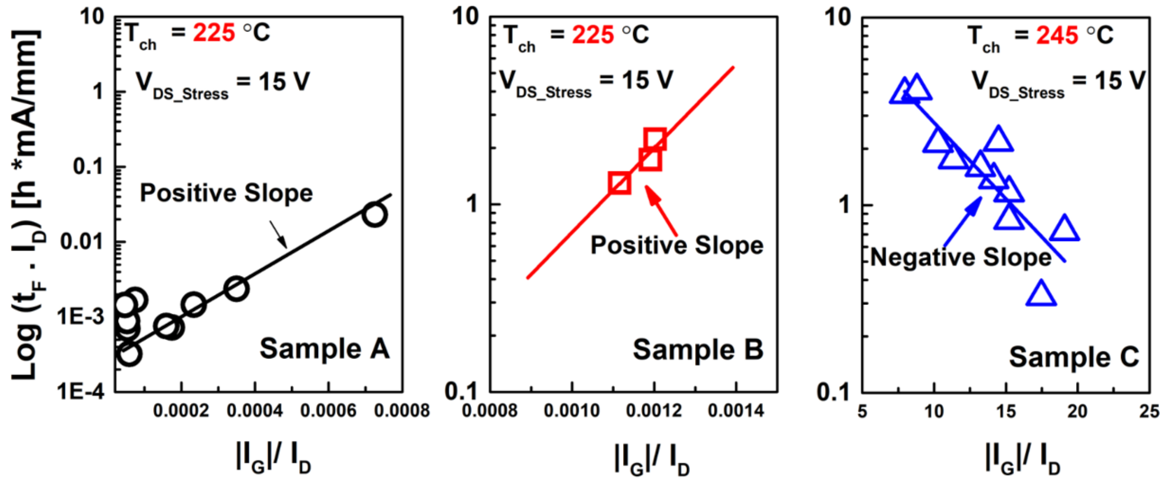


Figure 5.11 : Experimental (points) failure times multiplied by the stress drain current, versus the gate current over drain current ratio.

We estimated the MTTF values on wafer device perspective for all the samples. Figure 5.12 shows the MTTF values of sample A, B and C and the activation energy (E_v). At a temperature of 150°C, samples A and B show shorter mean-time-to-failure (MTTF) of 257 and 361 hours, respectively, due to their high leakage current (I_g) and increased on-resistance (R_{on}), whereas sample C displays a longer MTTF of 645 hours. Activation energies also calculated for each sample where the lowest MTTF value found in sample C, E_a = 0.47 eV. For sample A and B, it is found 0.55 eV and 0.52 eV respectively.

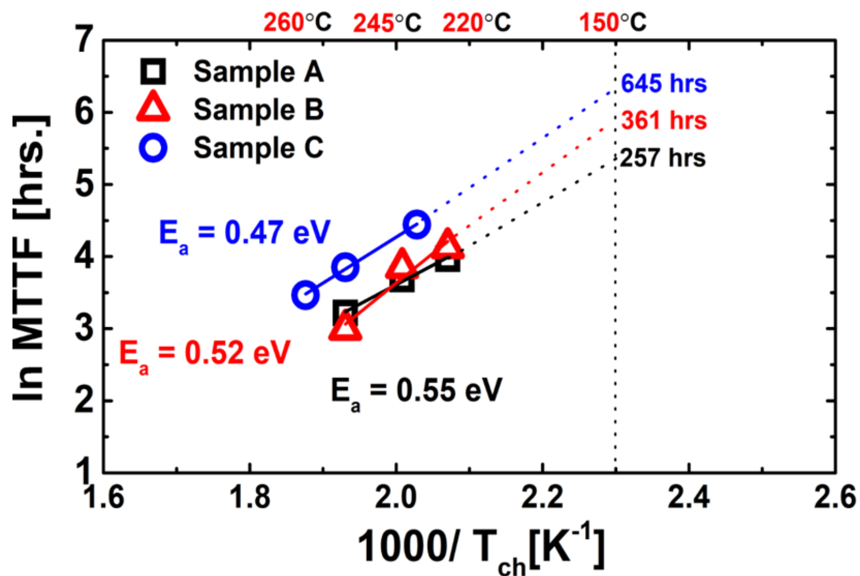


Figure 5.12 : MTTF values investigated for all the samples.

It is difficult to find accurately which degradation mechanisms are responsible only by seeing the activation energy. Different research groups estimated different activation energies for different kinds of mechanisms responsible for the degradation [47]. According to Kuball et. al, if the inter metal diffusion process has activation energy around 0.32 eV and the activation energy of 0.55 eV is related to hot-electron degradation [132].

5.4.1 Electrical Degradation : Sample A

The electrical degradation process of sample A is illustrated in Figure 5.13. When the device bias at high V_{DS} and $V_{GS} > V_{TH}$, the electron from channel layer (GaN) are subsequently trapped in the barrier layer and some portion of the electron can be trapped into the buffer layer also due to high electric field. These trapped electrons are modified the threshold voltage shift into the positive direction. Due to the thin barrier layer (8 nm), tunneling probability of the electrons are increased. Maximum number of electrons are trapped into the gate to drain access region and increased the lateral electric field (E_x). This whole phenomenon is related to Hot electron effect.

The fundamental concept is that electrons are initially injected into the AlGaN layer in the gate stack, possibly due to tunneling from the gate electrode under a high electric field. These injected electrons become trapped, resulting in a short-term positive shift in the threshold voltage (ΔV_T). The decrease in leakage current is associated with this phenomenon, although it might not be solely attributed to electron trapping in the AlGaN layer. Other factors, such as trapping occurring in or near the gate stack, could influence the barrier height and tunneling rate at the gate metal contact, thereby affecting the leakage current reduction.

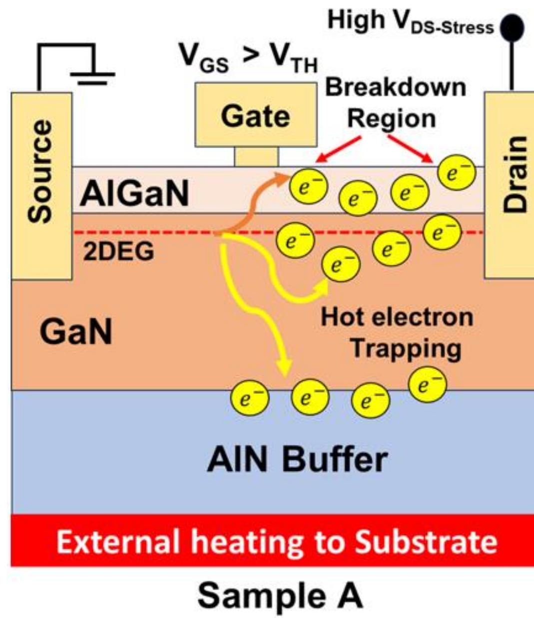


Figure 5.13: The physical mechanism behind breakdown of sample A where hot electrons trapped in the barrier and buffer layer result in G-D breakdown.

5.4.2 Electrical Degradation: Sample B

The degradation mechanism depicted on Figure 5.14. The main difference between sample A and B is inclusion of AlGaN back barrier (BB) and reduction of channel thickness. Due to the back barrier effect introduced by the AlGaN buffer, there is a substantial enhancement in the peak electric field near the gate edge on the drain side. This enhancement significantly contributes to the accelerated movement of electrons within the channel [142] These high-energy electrons will discharge the traps through a process known as hot electron emission. The physical mechanism of the breakdown is similar to sample A but introducing AlGaN/GaN BB suppress buffer leakage current that enhances the lifetime of the device.

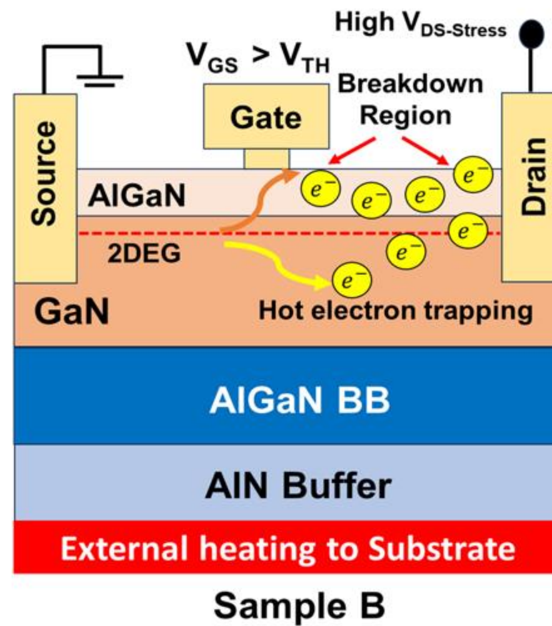


Figure 5.14: The physical mechanism behind breakdown of sample B. Due to the BB hot electron trapping occurs less in the buffer layer.

5.4.3 Electrical Degradation : Sample C

The breakdown mechanism of sample C is demonstrated in Figure 5.15. This structure is similar to conventional structure of GaN HEMTs but only the difference is doping of Carbon to achieve high resistive buffer. Buffer resistivity is a crucial design parameter for maximizing the breakdown voltage (V_{BD}) of AlGaN/GaN HEMTs. To control the resistivity of unintentionally n-type doped GaN buffers, iron (Fe) or carbon (C) doping is commonly employed. [143, 144]. Carbon (C) doping in the GaN buffer is widely acknowledged as an effective method to enhance the buffer's breakdown voltage. The behavior of carbon (C) in GaN is widely debated, as it is thought to act as an acceptor trap [145]. Additionally, it was observed that the breakdown voltage (V_{BD}) increased with an increase in the thickness of the C-doped GaN buffer [146]. As the concentration of acceptor traps increases (doping concentration of carbon in the buffer is near about 5×10^{18} cm^{-3} in sample C), the electric field near the drain side gate edge relaxes, causing the electric field peak to shift closer to the drain edge where the avalanche hot spot is observed. In addition to impacting buffer resistivity, acceptor traps in the GaN buffer can also introduce free holes into the GaN buffer and act as charged ions upon ionization.

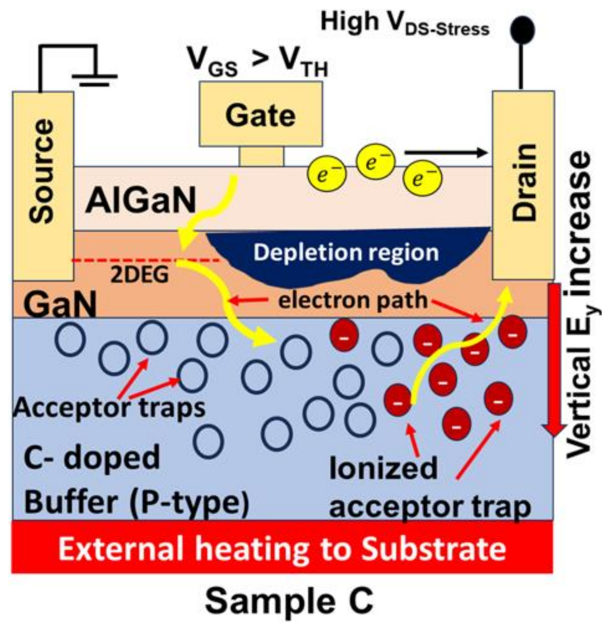


Figure 5.15: The physical mechanism behind breakdown of sample C. Carbon (C)-doped buffer induced acceptor trap ionization and vertical E_y increased.

The density of ionized acceptor traps represents the negative charge resulting from the trapping of an electron. These two factors have the potential to alter the space charge distribution across the GaN buffer and, consequently, may lead to a readjustment of the electric field. When acceptor traps ionize by capturing electrons from the 2-DEG, they generate a negative charge in the buffer region. Since these traps are situated beneath the drain electrode, an electric field forms between the positively biased drain electrode and the negatively charged acceptor ions. The peak of this electric field increases as the distance between the drain electrode and the region affected by the traps is reduced or if acceptor trap concentration is increased.

In accelerated life-time test, the device is under high temperature and high voltage stress. Due to high temperature, buffer traps will ionize through the process of hole emission. Furthermore, in conjunction with hot electron injection and trapping at the AlGaN interface and within the GaN buffer, this phenomenon can result in an expansion of the depletion region towards the drain electrode, ultimately leading to an increase in electric field intensity near the drain electrode.

Conversely, an increase in lattice temperature also accelerates the emission of trapped electrons, originating from surface and buffer traps. These emitted electrons tend to migrate towards the drain electrode due to the high V_{DS} stress. The breakdown is enhanced due to the increase in the vertical electric field.

5.5 Summary

In this chapter, we have explored the comparison between three HEMTs technologies and the underlying physics of electrical degradation of HEMTs in terms of long-term reliability assessment. To achieve high f_t and f_{max} , the epitaxial structure modification includes a lower AlGaN barrier thickness and a high Al% fraction, but in terms of long-term reliability, these epitaxial structures are not stable. For better stability and reduced buffer leakage current, buffer resistivity is required, which can be achieved by carbon (C) doping induced in the buffer layer. In addition, the electrical degradation mechanism is explained, which is generally affected by hot electron-induced traps and impact ionization. Therefore, for long-term stability and reliability, the optimization of the AlGaN barrier layer and a high-resistive buffer layer need to be implemented in future research.

Chapter 6

Conclusion

6.1 Summary

In this thesis, we have investigated the reliability issues in AlGaN/GaN HEMTs with different technologies. This work is a follow-up to our previous research, in which we investigated various fundamental degradation mechanisms that occur under electrical stress. In particular, our focus is on the hot electron effect and hot electron-induced impact ionization. We analyzed different models for the estimation of Mean-time-to-failure (MTTF). We systematically showed that only AlGaN/GaN HEMTs are affected by both electric field/voltage and temperature. Therefore, considering only temperature-related degradation is not meaningful for the estimation of MTTF for AlGaN/GaN HEMTs. Our analysis shows that AlGaN/GaN HEMTs have multiple degradation mechanisms depending on various voltage stress conditions. We proposed a hypothesis to calculate an acceleration factor that considers both temperature and voltage, named the combined acceleration factor.

On the other hand, we have discussed channel temperature determination, which has a significant impact on measuring MTTF estimation in the device. We have developed a new channel temperature model using an empirical expression that determines accurate predictions. The model is verified with experiments and Silvaco TCAD simulations.

To further investigate the influence of the electric field on long-term reliability, we tested the device under two distinct stress conditions: low electric field with high current and high electric field with low current. We observed that in low electric field stress, MTTF values are higher compared to high electric field stress.

To understand the mechanism of electrical degradation, we have conducted a detailed experiment on three distinct HEMT technologies. After HTOL testing and analysis of degradation parameters, we summarized that during On-stress testing, hot electrons and hot electron-induced impact ionization are the main mechanisms for electrical degradation.

6.2 Future Work

Our future work suggests improving device reliability by mitigating the hot electron effect in these devices. Although the highest f_t and f_{max} can be achieved by implementing a low barrier thickness of the AlGaN layer and a high Al% mole fraction, these devices suffer from long-term reliability issues and are prone to degradation.

On the other hand, optimizing the channel thickness is also an important parameter to consider, as a better-optimized channel can provide a more favorable electric field for the device. Additionally, including an AlGaN back barrier or a doped buffer layer, such as C or Fe doping, can reduce buffer leakage current. Therefore, we plan to investigate all possible options to minimize degradation and achieve high reliability in the future.

We have discussed mean-time-to-failure (MTTF) conducting DC stress, but in RF stress, it may be different, and the device is subjected to be more degraded under RF conditions. In future, MTTF under RF stress condition should be investigated.

The on-wafer devices that were investigated in this thesis have no passivation layer, the reliability as well as MTTF value can be increased if passivation of high-k dielectrics can be applied. Field plate technology must be applied for reduction of the lateral electric field in the edge of the gate side.

Moreover, for better reliability and high performance of the devices depends on the optimization of buffer layer and barrier layer. The thermos-mechanical issues in AlGaN/GaN HEMTs are also need to be examined properly for better reliability in future.

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AlGaN/GaN HEMTs 의

신뢰성 평가와 퇴화 물리학에 관한 연구

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질화 갈륨 고전자 이동성 트랜지스터(GaN HEMT) 기술의 광범위한 적용은 주로 전기적 신뢰성과 관련된 중대한 도전에 직면해 왔습니다. GaN HEMTs 는 다양한 전기 과부하 조건에 대해 놀라운 저항력을 보이지만, 그들의 장기 신뢰성을 보장하는 것이 중요한 고려사항으로 부상했습니다. 장치의 수명을 평가하는 핵심적인 매개변수인 평균 고장 시간(MTTF)은, 다양한 온도 조건에서 실시된 광범위한 장기 신뢰성 테스트에도 불구하고, 정확한 추정을 피해왔습니다. 이 박사 논문은 GaN HEMTs 에 대해 전기장 스트레스가 장기 신뢰성에 미치는 깊은 영향에 대한 포괄적인 탐구를 수행하였습니다. 이 논문은 소자의 퇴화를 뒷받침하는 복잡한 물리적 메커니즘을 깊이 파고들며, 주로 핫 전자에 의한 트랩 현상과 충격 이온화의 영향에 주목합니다. MTTF 값이 온도뿐만 아니라 특정 전기장 스트레스 조건에도 영향을 받음을 강조하면서, 이 연구는 이러한 퇴화 메커니즘과 그들의 보다 넓은 함의에 대한 깊은 이해를 제공하려고 합니다. 이러한 이해는 성능과 신뢰성을 모두 최적화하는 소자 구조의 의도적인 설계에 대한 토대를 제공합니다. 이러한 복잡한 문제를 풀어내기 위해, 고온 작동 수명(HTOL) 테스트 내에서 다양한

바이어스 조건 하에서 GaN HEMTs 의 중요한 매개변수인 드레인 전류 (I_{DS}), 문턱 전압 이동(ΔV_T), 트랜스 컨덕턴스(G_{max}), 온 저항(R_{on}), 게이트 누설 전류(I_{g_leak})의 퇴화에 대한 체계적인 분석이 수행됩니다. 전압과 온도를 모두 고려하는 복합 가속 요인의 독특한 제안은 정확한 MTTF 결정을 용이하게 하며, AlGaN/GaN HEMTs 가 전기장/전압과 온도 사이의 복잡한 상호 작용을 통해 신뢰성을 보여줌을 나타냅니다. 마지막으로, 핫 전자와 핫 전자에 의한 충격 이온화를 포함한 세 가지의 다른 HEMT 기술에 대한 심층적인 분석은, 이러한 메커니즘들이 On-stress 테스트 동안 주요하게 나타나며, 전기적 퇴화에 크게 기여함을 보여줍니다.