Three-phase Embedded Modified-Z-Source Three-Level T-Type Inverters

FOR THE DEGREE OF
MASTER OF SCIENCE

BY

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School of Electrical Engineering

Graduate School of University of Ulsan

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SUMMARY

Three-phase Embedded Modified-Z-Source Three-Level T-Type Inverters

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Two topologies are designed by combining a modified-Z-source impedance (MZS) network consisting of three diodes, two inductors and four capacitors to the traditional three-level T-type inverter (3LTI), and embedding either one or two dc sources in the impedance network, which are named as asymmetrical embedded MZS-3LTI (AEMZS-3LTI) and symmetrical embedded MZS-3LTI (SEMZS-3LTI). The proposed topologies provide a highly boosted ac output voltage with five voltage levels and ensure a continuous dc source current by adopting the embedded concept. In comparison to other topologies combining the impedance network and 3LTI, the proposed SEMZS-3LTI topology has two times higher boost factor and the lowest ratio of voltage stress across capacitors to the ac output voltage. The modulation technique is proposed for effectively controlling the upper and lower shoot-through states with a simple logic circuit and balancing two series capacitor voltages. The validity of the proposed topologies and the modulation technique is demonstrated through simulation and experimental results.

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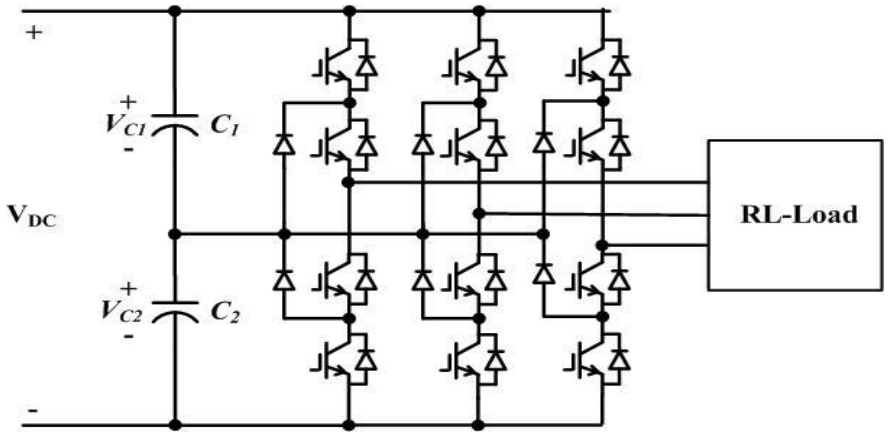
CHAPTER 1
INTRODUCTION

1.1 Background

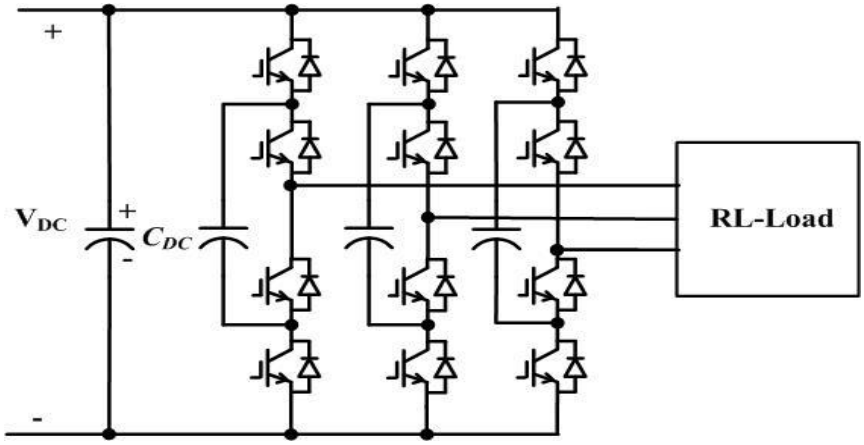
1.1.1 Multilevel inverters and three-level T-type inverter

Recently, multilevel inverters have been an effective solution in high-power applications such as the ac motor control [1] and the renewable energy generation systems [2], [3]. They can provide a lower total harmonic distortion (THD) due to a stepped output waveform more than two voltage levels and can reduce the voltage stress of the inverter switching devices, compared to a conventional two-level inverter. Among various multilevel topologies, the neutral-point-clamped (NPC), cascaded H-bride (CHB)[4], and flying capacitors (FC)[5] inverters, which are shown in Fig. 1, have been widely used.

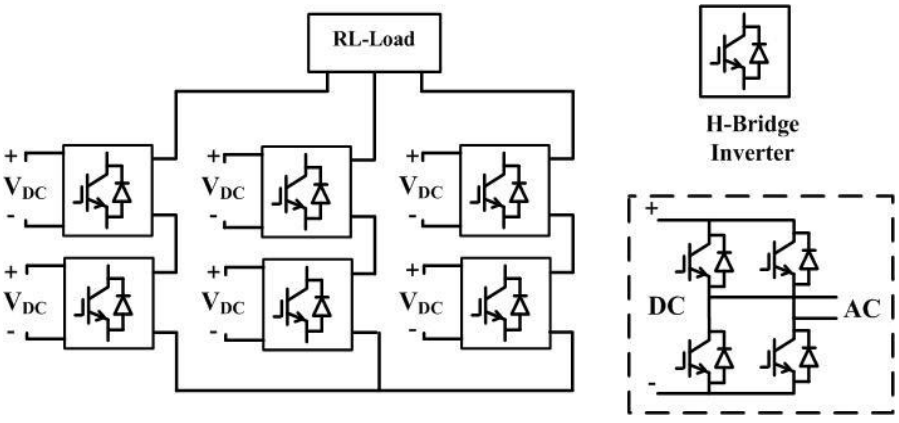
However, there are some disadvantages associative with three popular multilevel topologies. The CHB inverters require separate dc sources, and both the FC and NPC inverters suffer from the dc-link capacitor voltage unbalance. As a relatively recent three-level inverter topology, the three-level T-type inverter (3LTI) was introduced, which is implemented by connecting an active bidirectional switch between the dc-link midpoint and the three-phase outputs of the conventional two-level inverter as shown in Fig. 2 [6]-[15]. Compared to the three-phase three-level NPC inverter, it can provide lower conduction losses and a decreasing number of diodes while retaining the benefit of the three-level inverter such as the stepped output voltage waveform.



(a) Neutral-point-clamped (NPC) inverter



(b) Flying capacitors (FC) inverter



(c) Cascaded H-bride (CHB) inverter

Fig. 1. Three popularly three-level inverters.

In [6] and [7], the switching and conduction losses of 3LTI for low-voltage applications are analyzed and compared to three-level NPC inverter or two-level inverter. The fault-tolerant control strategies for a 3LTI under an open-circuit fault condition are proposed by measuring the bridge voltage or neutral-point voltage [8]-[11]. The 3LTI can be applied in various industrial applications such as PV generation [12], permanent-magnet synchronous motor (PMSM) drives [13], [14], and energy storage systems [15]. However, the 3LTI, as well as the three highly popular three-level topologies, perform only a buck dc-ac voltage conversion, because they are unable to output the ac voltage higher than dc source voltage. Therefore, 3LTI has serious trouble to apply some applications like a renewable energy generation with a low voltage renewal energy source, which demands the 3LTI with a higher voltage gain to obtain a desired ac output voltage.

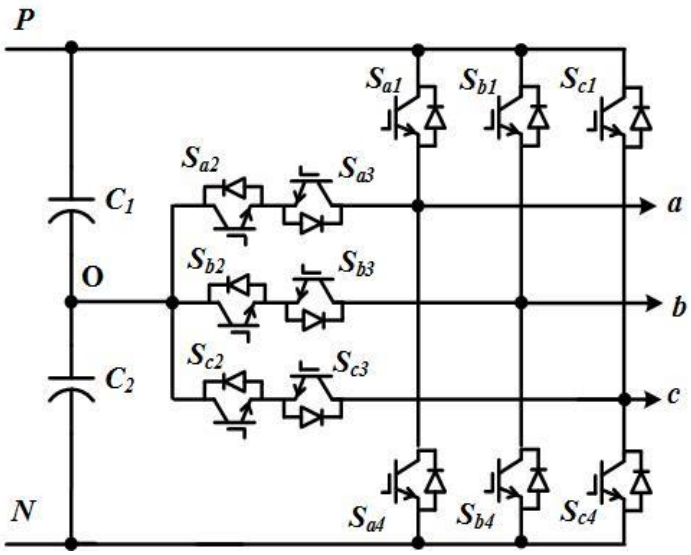
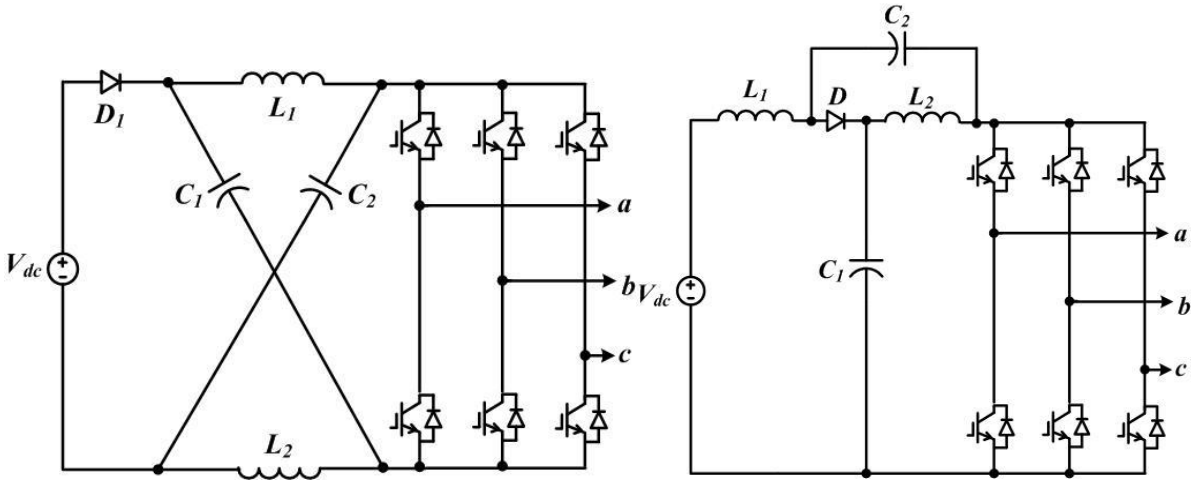


Fig. 2. Structure of three-phase three-level T-type inverter.

1.1.2 Z-source and quasi-Z-source impedance network

In order to enhance the boost ability of 3LTI with a single power conversion stage, the (quasi)-Z-source impedance network concept is applied to the 3LTI. Fig.3 illustrates the Z-source inverter (ZSI) and quasi-Z-source inverter (qZSI).



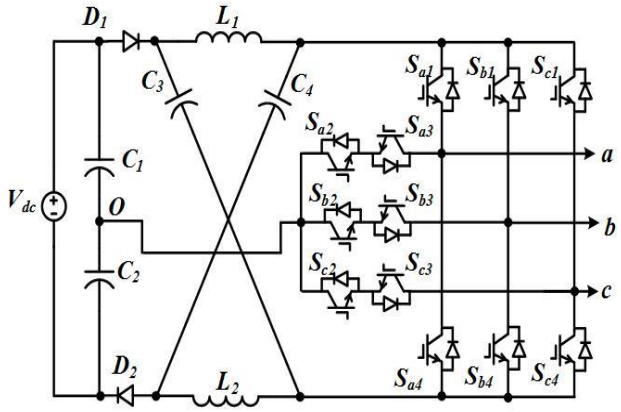
(a) ZSI (b) qZSI

Fig. 3. Structure of ZSI and qZSI.

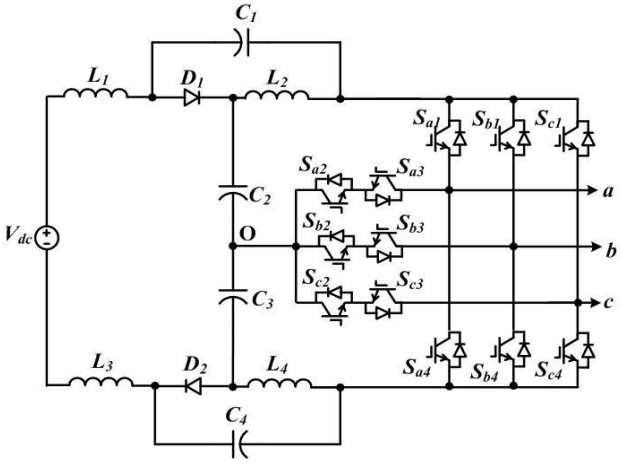
The basic concept of the ZSI has been introduced by Prof. F. Z. Peng [16]. The ZSI allows that the load terminals are shorted through both the upper and the lower switching devices of any phase leg of the inverter [17]-[18]. The ZSI has one more switching state compared to the traditional three-phase voltage-source inverter. The boost ability can be achieved by the extra shoot-through state which is forbidden at the traditional inverter due to short-circuit. A buck-boost operation can be achieved with a single power conversion stage. Because the dead-time of the inverter is not necessary, the reliability is improved.

The qZSI provides a continuous dc source current and a lower capacitor voltage stress, and it has a common dc rail between the dc source and inverter which can solve EMI problems. The boost ability of qZSI is the same as that of the ZSI. [19]

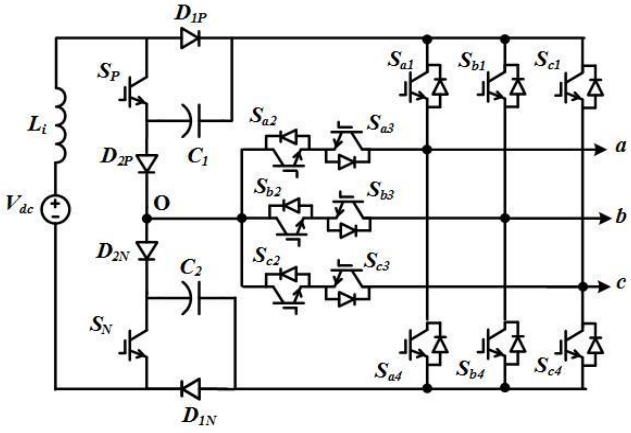
1.1.3 Topologies combining (quasi)-Z-source impedance and 3LTI



(a) ZS-3LT^{2}I



(b) qZS-3LT^{2}I



(c) 3L-qSBT^{2}I

Fig. 4. Three different topologies combining impedance network and 3LTI.

Several topologies integrating the (quasi-)Z-source impedance network to the 3LTI have been proposed, in order to get the benefits of (q-)ZSI as well as those of the 3LTI.

The topology and modulation method for the three-phase or single-phase Z-source three-level T-type inverters (ZS-3LT^{2}I), which are implemented by combining a single Z-source impedance and three- or single-phase 3LTI are described, respectively, in [20], [21]. Fig. 4(a) shows the structure of the ZS-3LT^{2}I, which has a discontinuous dc source current. The space vector modulation scheme and the carrier level shifted modulation method of the quasi-Z-source three-level T-type inverters (qZS-3LT^{2}I) topology, realized by combining the two symmetrical quasi-Z-source networks and three-phase 3LTI as shown in Fig. 4(b), are proposed in order to reduce the common-mode voltage by balancing the neutral-point voltage [22]-[24]. The behaviors for the normal operation and open-loop failure condition of the qZS-3LTI are studied in [25]. An efficiency study to compare the qZS-3LT^{2}I and qZS-NPC inverter is realized by simulations [26]. The qZS-3LT^{2}I has a continuous source current. However, it requires a large number of passive components, which results in increasing the weight, volume, and cost of the power converter. Although both the ZS-3LTI and qZS-3LTI have a boost capability, their boost factor is not high.

In order to improve the boost capability while reducing the number of passive components, the three-level quasi-switched boost T-type inverter (3L-qSBT^{2}I) topology is introduced in [27]-[29]. The 3L-qSBT^{2}I topology is designed by replacing the quasi-Z-source impedance network in the qZS-3LTI to the quasi-switched boost network proposed in [30], [31] where it consists of one inductor, two capacitors, four diodes, and two active switches, as shown in Fig. 4(c). The 3L-qSBT^{2}I topology can provide a high voltage gain and reduce the number of passive components. However, it requires two additional switching devices and a complex modulation technique. An active impedance-source 3LTI with reduced component count (RC^2-AIS-3LTI) topology is introduced in order to reduce the count of the active and passive switches [32]. It can save two diodes and one active switch, compared to the 3L-qSBT^{2}I topology.

1.2 Objectives and scope of the thesis

In this thesis, the three-phase embedded modified-Z-source three-level T-type inverter topologies are introduced. The proposed topologies are designed by attaching a single modified-Z-source impedance (MZS) network proposed in [33] to the 3LTI, and embedding one dc source or two dc sources at the MZS impedance network, which are named as an asymmetrical embedded MZS-3LTI (AEMZS-3LTI) and symmetrical embedded MZS-3LTI (SEMZS-3LTI), respectively. They can improve the boost ability and ensure the continuous dc source current without any extra capacitor or filter by employing the embedded concept. The operations for the shoot-through and non-shoot-through states of both the AEMZS-3LTI and SEMZS-3LTI are analyzed, respectively. A novel modulation technique based on an alternative phase opposition disposition (APOD) for the proposed topologies is proposed in order to produce the boosting ac output voltage with five voltage steps. The performances of the proposed topologies and modulation techniques are demonstrated through simulation and experimental results.

1.3 Overview of Thesis

The thesis is organized as follows:

Chapter 1 introduces the background knowledge about the multilevel inverters, (quasi-)Z-source inverters. Then, the characteristics of some relative topologies combining the impedance network and 3LTI are discussed. The asymmetrical embedded MZS-3LTI (AEMZS-3LTI) and symmetrical embedded MZS-3LTI (SEMZS-3LTI) are introduced, and the objectives and the scope of the thesis are also described.

Chapter 2 introduces the main contributions of the thesis. The chapter analyzes the operations of proposed AEMZS-3LTI and SEMZS-3LTI topologies.

Chapter 3 compares the two proposed topologies to three different topologies combining the impedance network and 3LTI.

Chapter 4 shows the novel modulation technique to generate a boosted ac output voltage by adjusting effectively the shoot-through states.

Chapter 5 shows the simulation results of the two proposed topologies.

Chapter 6 shows the experimental setup configuration and experimental results of the two proposed topologies.

Chapter 7 discusses the main contributions of this thesis.

CHAPTER 2

OPERATION ANALYSIS OF ASYMMETRICAL EMZS-3LTI & SYMMETRICAL EMZS-3LTI

2.1 Operating principles of AEMZS-3LTI

Fig. 5 shows the structure of the proposed AEMZS-3LTI, which is designed by combining the MZS network [33] and the 3LTI, and placing a single dc source in serial with the inductor L_1 of the upper cell in the impedance network [34]. The operation analysis for the proposed AEMZS-3LTI topology is performed, assuming that all of the components adopted at the proposed topology are ideal for simplification. The MZS network contains three diodes, two inductors, and four capacitors. The continuous dc source current can be achieved without any additional filter or capacitor. Three-phase bidirectional active switches are connected between the mid-point of two serial capacitors C_1 and C_2 and the three-phase outputs of the two-level inverter.

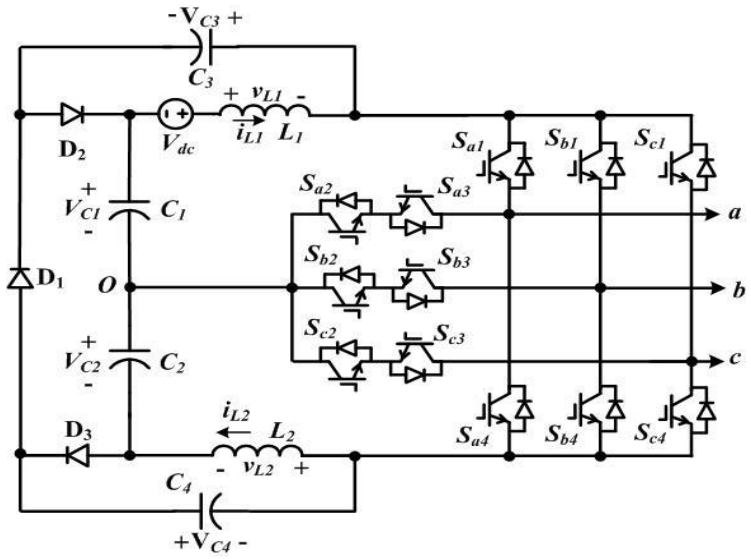


Fig. 5. Structure of three-phase AEMZS-3LTI topology.

The operating state of the proposed topology can be divided into the shoot-through state and the non-shoot-through (NST) state like traditional ZSI. The equivalent circuits for both operating states are described, in order to perform a steady-state analysis of the operations of the proposed topology.

We assume that $C_1 = C_2 = C_3 = C_4$ and $L_1 = L_2$.

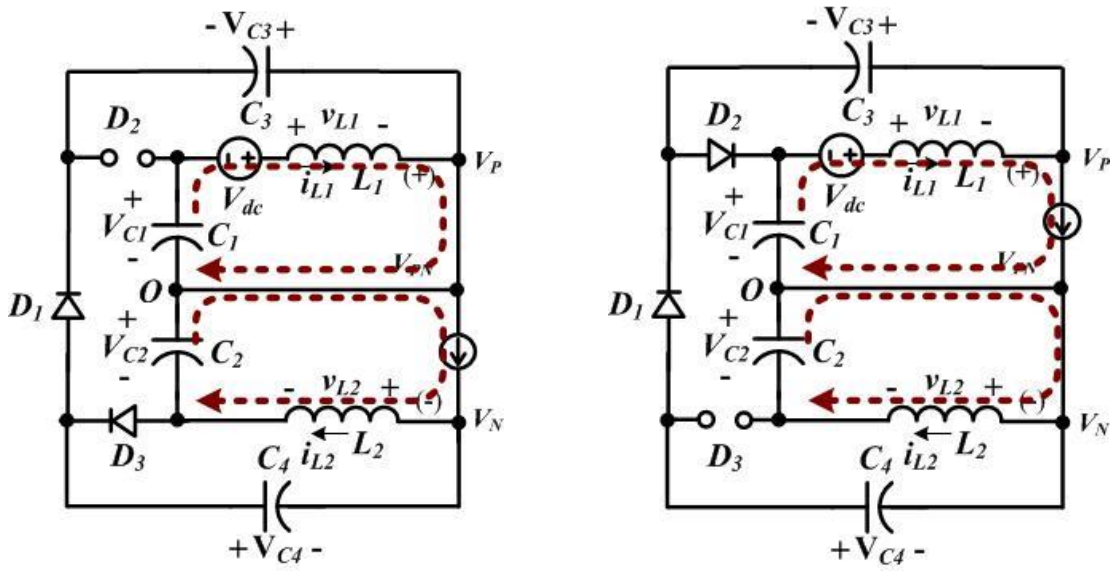
Because of the symmetrical characteristic of the impedance network, it can be assumed that $V_{C1} = V_{C4}$ and $V_{C2} = V_{C3}$ due to the MZS network [34].

2.1.1 Shoot-through state

Three types of shoot-through states such as a full shoot-through (FST) state, an upper shoot-through (UST) state and a lower shoot-through (LST) state are available at the three-phase AEMZS-3LTI.

In FST state, the voltage across a full dc-link of the inverter becomes zero by conducting the upper and lower switches in any phase leg. The zero output voltage during FST state may cause a distorted output voltage. Both the upper and lower shoot-through states can be made by conducting the upper or lower switch and the bidirectional switches. Because the output voltage can be produced during both the UST and LST states, it can be achieved to improve the quality of the output voltage waveform.

Fig. 6 shows the equivalent circuits in the UST and LST states for the three-phase AEMZS-3LTI.



(a) UST state (b) LST state

Fig. 6. Equivalent circuits of shoot-through states for three-phase AEMZS-3LTI.

a) Upper shoot-through (UST) state

In the UST state, the short circuit condition of the upper impedance cell can be made by turning on switches S_{x1}, S_{x2}, and S_{x3} (x = a, b, or c), as shown in Fig. 6(a). Two diodes D_1 and D_3 are conducting, whereas diode D_2 is blocking. Both the dc input source and the capacitor C_1 delivery energy to the energy to the inductor L_1. Both the inductor L_2 and capacitor C_2 supply energy to the load side. From the Fig.6(a), the two inductor voltages V_{L1} and V_{L2} can be written by

$$V_{L1} = V_{C1}+V_{dc} \tag{1}$$

$$V_{L2} = -V_{C4.} \tag{2}$$

The dc-link voltage V_{PN} can be written by

$$V_{PN} = V_{C2}+V_{C4.} \tag{3}$$

b) Lower shoot-through (LST) state

In the LST state, the short circuit condition of the lower impedance cell can be made by turning on switches S_{x2} and S_{x3}, and S_{x4} (x = a, b, or c), as shown in Fig. 6(b). Two diodes D_1 and D_2 are conducting, whereas diode D_3 is blocking state. The inductor L_2 charges the energy from the capacitor C_2 at the lower impedance cell. Two capacitors C_1 and C_3 delivery energy to the ac load side.

From the Fig. 6(b), the two inductor voltages V_{L1} and V_{L2} can be written by

$$V_{L1} = -V_{C3} + V_{dc} \tag{4}$$

$$V_{L2} = V_{C2}\,. \tag{5}$$

The dc-link voltage V_{PN} can be written by

$$V_{PN} = V_{C1} + V_{C3}\,. \tag{6}$$

2.1.2 Non-shoot-through state

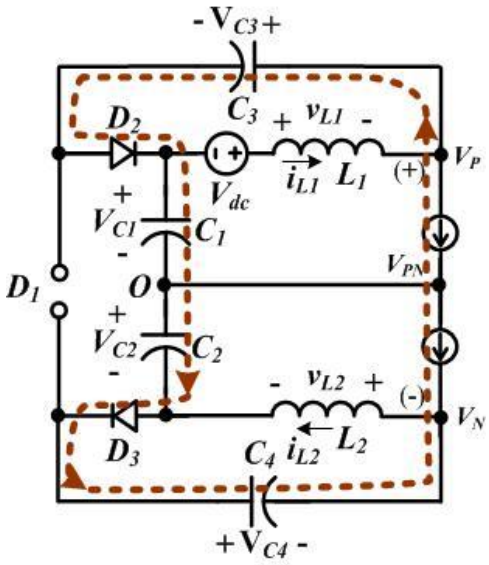


Fig. 7. Equivalent circuit of non-shoot-through state for three-phase AEMZS-3LTI.

Fig. 7 shows the equivalent circuit of the NST state, which can be divided into an active state and a zero state. The AEMZS-3LTI operates like the traditional 3LTI. The diodes D_2 and D_3 are conducting whereas diode D_1 is blocking. The switches S_{x1} and S_{x2} are turned on at the positive x-phase reference signal, and the switches S_{x3} and S_{x4} are turned on at the negative x-phase reference signal during the active state.

The two inductor voltages V_{L1} and V_{L2} can be written by

$$V_{L1} = -V_{C3} + V_{dc} \tag{7}$$

$$V_{L2} = -V_{C4}\,. \tag{8}$$

The dc-link voltage V_{PN} can be written by

$$V_{PN} = V_{C1} + V_{C2} + V_{C3} + V_{C4}\,. \tag{9}$$

2.1.3 Boost factor

The average values of UST and LST periods are the same over one period of the inverter frequency due to the symmetrical operation of the modulation technique. Therefore, the period of UST and LST is represented as T_{ST}.

Assuming $V_{C1} = V_{C4}$ and $V_{C2} = V_{C3}$, the four capacitor voltages are expressed as a function of the shoot-through duty ratio D, which is defined as $D = T_{ST}/T$. By utilizing the voltage-second balance principle to inductors L_1 from (1), (4), and (7) over one switching period T, we obtain

$$(V_{C1} + V_{dc})D + (-V_{C3} + V_{dc})D + (-V_{C3} + V_{dc})(1-2D) = 0$$

$$<=> \qquad V_{C1}D + V_{C3}(D-1) + V_{dc} = 0\,. \tag{10}$$

From (10), the relationship between the voltages on C_1 and C_3 can be given as

$$V_{C1} = \frac{1}{D}[V_{C3}(1-D) - V_{dc}] = V_{C4}. \tag{11}$$

By utilizing the voltage-second balance principle to inductors L_2 from (2), (5), and (8) over one switching period T, we obtain

$$V_{C4}D + V_{C2}D - V_{C4}(1-2D) = 0$$

$$<=> \qquad V_{C4} = \frac{D}{(1-D)}V_{C2}\,. \tag{12}$$

The four capacitor voltages are expressed as a function of the shoot-through duty ratio D

$$V_{C2} = V_{C3} = \frac{1-D}{1-2D}V_{dc} \tag{13}$$

$$V_{C1} = V_{C4} = \frac{D}{1-2D}V_{dc}\,. \tag{14}$$

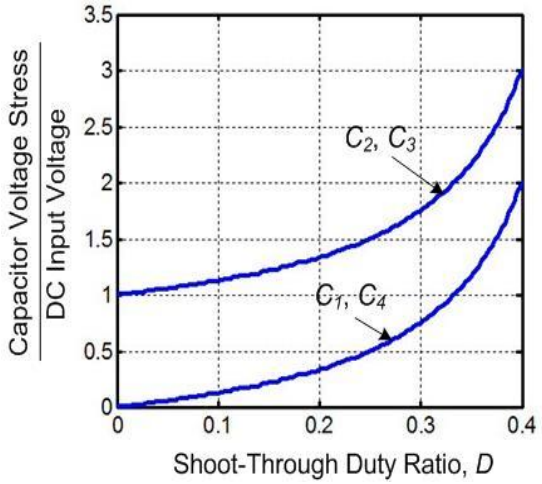


Fig. 8. Capacitor voltage stress with a variation of the shoot-through duty ratio.

Fig. 8 shows the plots of the four capacitor voltages to the dc input voltage with a variation of D. The voltage stress of two capacitors C_2 and C_3 is higher than that of two capacitors C_1 and C_4.

By substituting (13) and (14) into (9), the boost factor B, defined as the ratio of the peak dc-link voltage to the dc input voltage is given by

$$B = \frac{\hat{V}_{PN}}{V_{DC}} = \frac{2}{1-2D}. \tag{15}$$

The overall dc-ac voltage gain G is defined as

$$G = \frac{\hat{v}_o}{(V_{dc}/2)} = \frac{2\sqrt{2}\,V_{o(rms)}}{V_{dc}} = M.B \tag{16}$$

where: $\hat{v}_o$ is the peak output phase voltage

$M=(1-D$ is the modulation index.

From (15) and (16), the rms value of the output voltage can be derived as

$$V_{o(rms)} = \sqrt{2}\frac{1-D}{1-2D}V_{dc}. \tag{17}$$

2.2 Operating principles of SEMZS-3LTI

Fig. 9 shows the structure of the proposed SEMZS-3LTI topology, which is designed by combining the MZS network and the 3LTI, and placing two dc sources V_{dc1} and V_{dc2} at the upper and lower cells in the MZS network, respectively. The MZS network contains three diodes, two inductors, and four capacitors. The continuous dc source current can be achieved without any additional filter or capacitor as in the AEMZS-3LTI. Three-phase bidirectional active switches are connected between the mid-point of two serial capacitors C_1 and C_2 and the three-phase outputs of the two-level inverter.

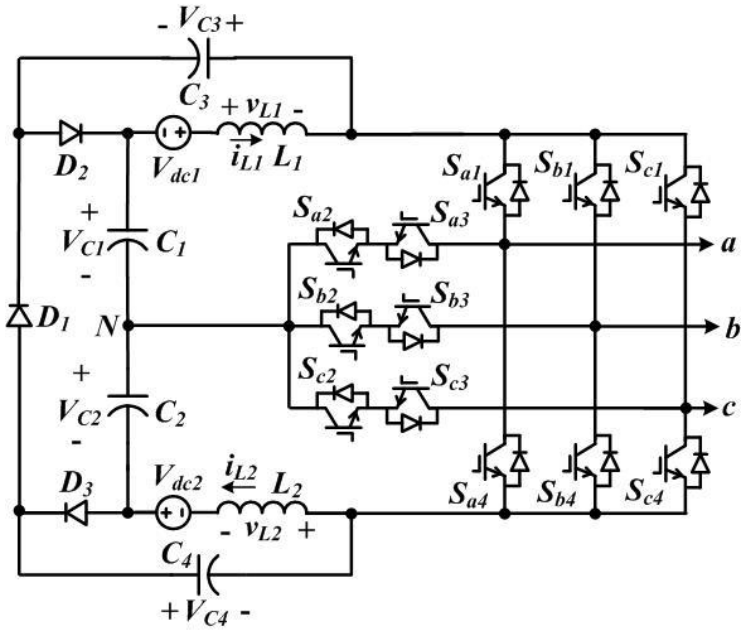


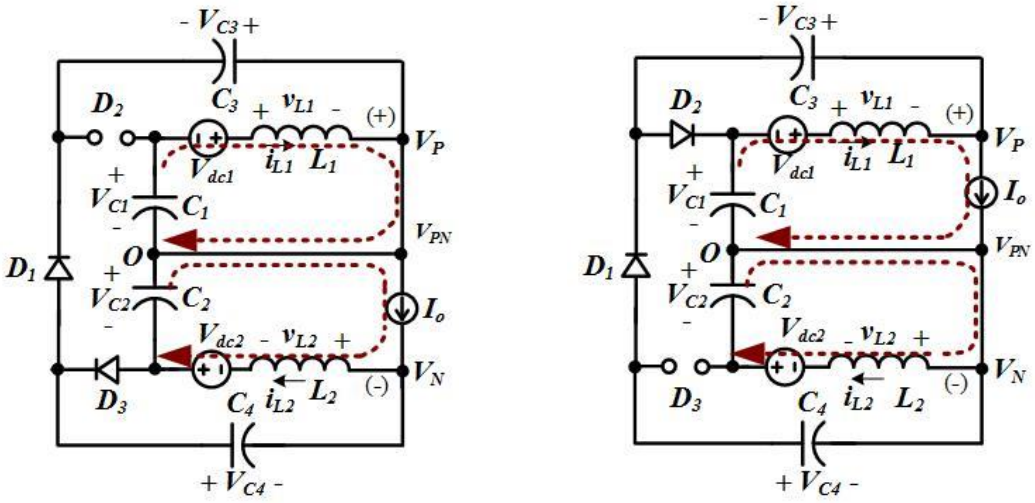
Fig. 9. Three-phase SEMZS-3LTI topology.

The operating state of the proposed topology also can be divided into the shoot-through state and the non-shoot-through (NST) state like traditional ZSI. The on/off switching devices and dc-link voltage of the SEMZS-3LTI topology are the same as those of the AEMZS-3LTI topology in all three operating states.

We assume that $C_1 = C_2 = C_3 = C_4$ and $L_1 = L_2$. Because of the symmetry of the impedance network, it can be assumed $V_{C1} = V_{C2} = V_{C3} = V_{C4}$.

2.2.1 Shoot-through state

Three types of shoot-through states such as a full shoot-through (FST) state, an upper shoot-through (UST) state and a lower shoot-through (LST) state are available at the three-phase SEMZS-3LTI.



(a) UST state (b) LST state

Fig. 10. Equivalent circuits of shoot-through states for three-phase SEMZS-3LTI.

In FST state, the voltage across a full dc-link of the inverter becomes zero by conducting the upper and lower switches in any phase leg. The zero output voltage during FST state may cause a distorted output voltage. Both the upper and lower shoot-through states can be made by conducting the upper or lower switch and the bidirectional switches. Because the output voltage can be produced during both the UST and LST states, it can be achieved to improve the quality of the output voltage waveform.

a) Upper shoot-through state

In the UST state shown in Fig.10 (a), both the dc input source V_{dc1} and the capacitor C_1 delivery energy to the inductor L_1. The dc input source V_{dc2}, the inductor L_2, and capacitor C_2 supply energy to the ac load side. The two inductors voltages V_{L1} and V_{L2} can be written by

$$V_{L1} = V_{C1} + V_{dc1} \tag{18}$$

$$V_{L2} = V_{dc2} - V_{C4}. \tag{19}$$

The capacitor currents can be written by

$$i_{C1} = - i_{L1}, \quad i_{C4} = i_{L2} - I_O. \tag{20}$$

b) Lower shoot-through state

In the LST state shown in Fig.10 (b), both the dc input source V_{dc2} and the capacitor C_2 deliver energy to the inductor L_2. The dc input source V_{dc1}, the inductor L_1, and capacitor C_1 supply energy to the ac load side. The two inductor voltages V_{L1} and V_{L2} can be written by

$$V_{L1} = V_{dc1} - V_{C3} \tag{21}$$

$$V_{L2} = V_{dc2} + V_{C2}. \tag{22}$$

The capacitor currents can be written by

$$i_{C2} = - i_{L2}, \quad i_{C3} = i_{L1} - I_O . \tag{23}$$

2.2.2 Non-shoot-through state

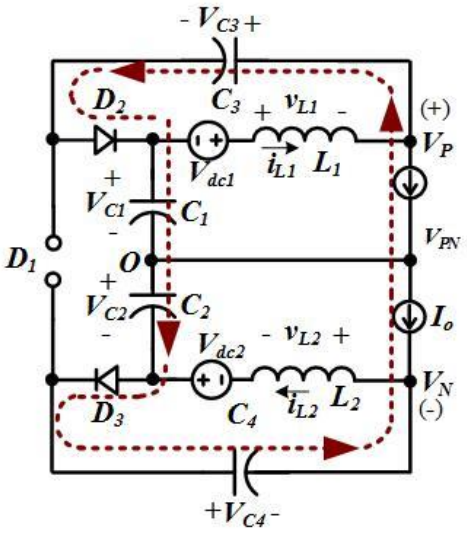


Fig. 11. Equivalent circuit of non-shoot-through for three-phase SEMZS-3LTI.

Fig. 11 shows the equivalent circuit of the NST state. In the active state, the switching states for *x*-phase four switching devices are dependent on the polarity of the *x*-phase reference signal and the dc-link voltage is a peak dc-link voltage as in the AEMZS-3LTI topology.

From the Fig.11, the voltages across inductors are given by

$$V_{L1} = V_{dc1} - V_{C3} \tag{24}$$

$$V_{L2} = V_{dc2} - V_{C4}\,. \tag{25}$$

The capacitor currents are given by

$$i_{C3} = i_{L1} - I_O \;,\; i_{C4} = -i_{L2} + I_O. \tag{26}$$

2.2.3 Boost factor

The average values of UST and LST periods are the same over one period of the inverter frequency due to the symmetrical operation of the modulation technique. Therefore, the period of UST and LST is represented as T_{ST}. Assuming $V_{C1} = V_{C2} = V_{C3} = V_{C4}$, the four capacitor voltages are expressed as a function of the shoot-through duty ratio D, which is defined as $D = T_{ST}/T$.

By utilizing the voltage-second balance principle to inductors L_1 from (18), (21), and (24) over one switching period T, we obtain

$$(V_{C1} + V_{dc1})D + (-V_{C3} + V_{dc1})D + (-V_{C3} + V_{dc1})(1-2D) = 0. \tag{27}$$

By utilizing the voltage-second balance principle to inductors L_2 from (19), (22), and (25) over one switching period T, we obtain

$$(V_{dc2} - V_{C4})D + (V_{in2} + V_{C4})D + (V_{in2} - V_{C4})(1-2D) = 0. \tag{28}$$

By using (27) and (28), the four capacitor voltages are expressed as a function of the shoot-through duty ratio D

$$V_{C1} = V_{C2} = V_{C3} = V_{C4} = \frac{1}{(1-2D)} V_{dc}. \tag{29}$$

By applying the charge-second balance principle to capacitors from (20), (23), and (26) over one switching period T, assuming $i_{C1} = i_{C2} = i_{C3} = i_{C4}$ and $i_{L1} = i_{L2}$, the averages of two inductor currents are obtained as

$$\overline{i}_{L1} = \overline{i}_{L2} = I_O. \tag{30}$$

The peak value of dc-link voltage $\hat{V}_{PN}$ can be written by

$$V_{PN} = V_{C1} + V_{C2} + V_{C3} + V_{C4}. \tag{31}$$

Substituting (29) into (31), the boost factor B is derived as

$$B = \frac{\hat{V}_{PN}}{V_{dc}} = \frac{4}{1-2D}. \tag{32}$$

The rms value of the output voltage can also be derived as

$$V_{o(rms)} = 2\sqrt{2}\ \frac{1-D}{1-2D}\ V_{dc}. \tag{33}$$

It can be seen that the boost factor of the SEMZS-3LTI topology is two times higher than that of the AEMZS-3LTI topology. Table.1 describes the output phase terminal voltages V_{Px} and V_{Nx} (x = a, b, or c) and the turn-on switching devices and diodes according to the operating states of the two proposed topologies.

Table. 1. Switching states of the two proposed topologies (x = a, b, or c)

State Type	ON switches	ON diodes	V_{Px}	V_{Nx}
UST	S_{1x}, $S_{2x,}$, S_{3x}	D_1, D_3	0	-(V_{C2}+V_{C4})
LST	S_{2x}, S_{3x}, S_{4x}	D_1, D_2	V_{C1}+V_{C3}	0
NST	(S_{1x}, S_{2x}) or (S_{3x}, S_{4x})	D_2, D_3	V_{C1}+V_{C3}	-(V_{C2}+V_{C4})
NST	S_{2x}, S_{3x}	D_2, D_3	0	0

CHAPTER 3
COMPARISON WITH OTHER TOPOLOGIES COMBINING IMPEDANCE NETWORK AND 3LTI

The proposed AEMZS-3LTI and SEMZS-3LTI topologies are compared to other topologies combining the impedance network and 3LTI such as the ZS-3LT^{2}I [20], the qZS-3LT^{2}I [22], and the 3L-qSBT^{2}I [27].

3.1 Comparison of the boost factor

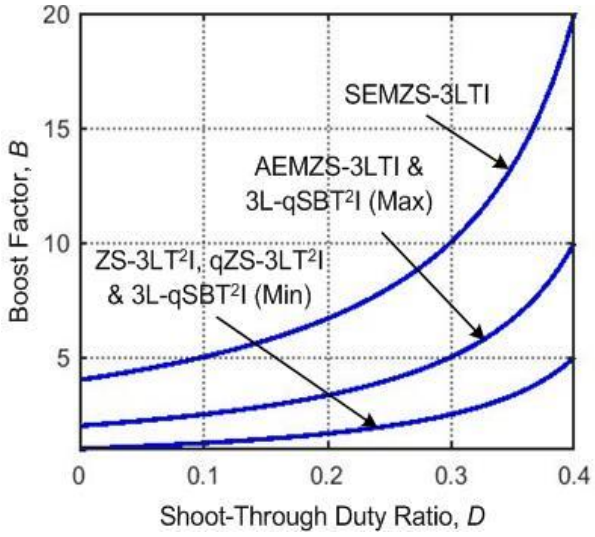


Fig. 12. Boost factor with a variation of *D*.

Fig. 12 shows plots of the boost factors of the two proposed topologies and three different topologies. Both the ZS-3LT^{2}I and qZS-3LT^{2}I have the lowest boost factor, and the boost factor of the 3L-qSBT^{2}I varies in the range of the lowest value and twice the lowest value. The boost factor of the SEMZS-3LTI is twice or four times higher than that of the three different topologies.

3.2 Comparison of the number of components

Table. 2 summarizes the number of passive and active components used at the impedance network. Compared to the ZS-3LT^{2}I, the proposed topologies require two more diodes. However, the ZS-3LT^{2}I has a discontinuous dc source current. Compared to the qZS-3LT^{2}I, the proposed topologies can use two fewer inductors and one additional diode and dc source (in the case of SEMZS-3LTI). In comparison to the proposed topologies, the 3L-qSBT^{2}I uses fewer inductors and capacitors. However, it needs one more diode and two additional active switches.

Table. 2. Number of components used in impedance network

	ZS-3LT^{2}I	qZS-3LT^{2}I	3L-qSBT^{2}I	AEMZS-3LTI	SEMZS-3LTI
Inductors	2	4	1	2	2
Capacitors	4	4	2	4	4
Diodes	1	2	4	3	3
Additional switches	0	0	2	0	0
DC sources	1	1	1	1	2

3.3 Comparison of capacitor voltage stress

In [20], [22], [27], the rms value of the output voltage of ZS-3LT^{2}I, qZS-3LT^{2}I and 3L-qSBT^{2}I (Min) topologies can be derived by

$$V_{o(rms)} = \frac{1}{\sqrt{2}} \frac{1-D}{1-2D} V_{dc}. \tag{34}$$

The rms value of the output voltage of 3L-qSBT^{2}I (Max) topology can be also derived by

$$V_{o(rms)} = \sqrt{2}\frac{1-D}{1-2D}V_{dc}. \tag{35}$$

Table. 3 shows the voltage stress across the capacitors in the impedance networks of the five topologies.

Table. 3. Comparison of voltage stress across the capacitors

ZS-3LT^{2}I		qZS-3LT^{2}I		3L-qSBT^{2}I		AEMZS-3LTI		SEMZS-3LTI	
C_1, C_2	$\frac{1}{2}$	C_1, C_4	$\frac{D}{2(1-2D)}V_{dc}$	C_P, C_N (Max)	$\frac{1}{1-2D}V_{dc}$	C_1, C_4	$\frac{D}{1-2D}V_{dc}$	C_1, C_2	$\frac{1}{1-2D}V_{dc}$
C_3, C_4	$\frac{1-D}{1-2D}V_{dc}$	C_2, C_3	$\frac{1-D}{2(1-2D)}V_{dc}$	C_P, C_N (Min)	$\frac{1}{2(1-2D)}V_{dc}$	C_2, C_3	$\frac{1-D}{1-2D}V_{dc}$	C_3, C_4	

To achieve a fair comparison of the capacitor voltage stresses for five topologies, the ratio of voltage stress across the capacitor to the rms value of ac output voltage is adopted to consider the cost to produce the desired output voltage. From (17), (33), (34), (35) and the Table.3, the ratio of voltage stress across capacitors to the rms value of the ac output voltage for the five topologies are calculated and described in Table. 4.

Table. 4. Comparison of capacitor voltage stress ratio

ZS-3LT^{2}I		qZS-3LT^{2}I		3L-qSBT^{2}I		AEMZS-3LTI		SEMZS-3LTI	
C_1, C_2	$\frac{1}{\sqrt{2}}\frac{1-2D}{1-D}$	C_1, C_4	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$	C_P, C_N	$\frac{1}{\sqrt{2}}\frac{1}{1-D}$	C_1, C_4	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$	C_1, C_2	$\frac{1}{2\sqrt{2}}\frac{D}{1-D}$
C_3, C_4	$\sqrt{2}$	C_2, C_3	$\frac{1}{\sqrt{2}}$			C_2, C_3	$\frac{1}{\sqrt{2}}$	C_3, C_4	

Fig. 13 shows the plots of capacitor voltage stress for five topologies. As shown in Fig. 13, the ratios of voltage stress across four capacitors of the proposed AEMZS-3LTI are identical with

those of the qZS-3LT^{2}I. The four capacitors of the proposed SEMZS-3LTI have the lowest voltage stress ratio.

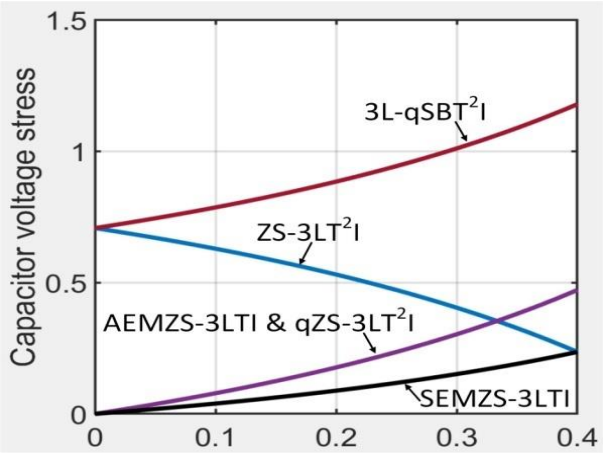


Fig. 13. Capacitor voltage stress with a variation of *D*.

3.4 Comparison of diode voltage stress

Table. 5 shows the diode voltage stress in the impedance networks of the five topologies. Both the ZS-3LT^{2}I and qZS-3LT^{2}I have the lowest diode voltage stress and the proposed SEMZS-3LTI topology has the highest diode voltage stress.

Table. 5. Comparison of diode voltage stress

ZS-3LT^{2}I (D_1, D_2)	qZS-3LT^{2}I (D_1, D_2)	3L-qSBT^{2}I (Max) (D_1, D_2, D_3, D_4)	AEMZS-3LTI (D_1, D_2, D_3)	SEMZS-3LTI (D_1, D_2, D_3)
$\frac{1}{2(1-2D)}V_{dc}$	$\frac{1}{2(1-2D)}V_{dc}$	$\frac{1}{1-2D}V_{dc}$	$\frac{1}{1-2D}V_{dc}$	$\frac{2}{1-2D}V_{dc}$

CHAPTER 4

MODIFIED MODULATION TECHNIQUE

4.1 Switching patterns for both proposed topologies

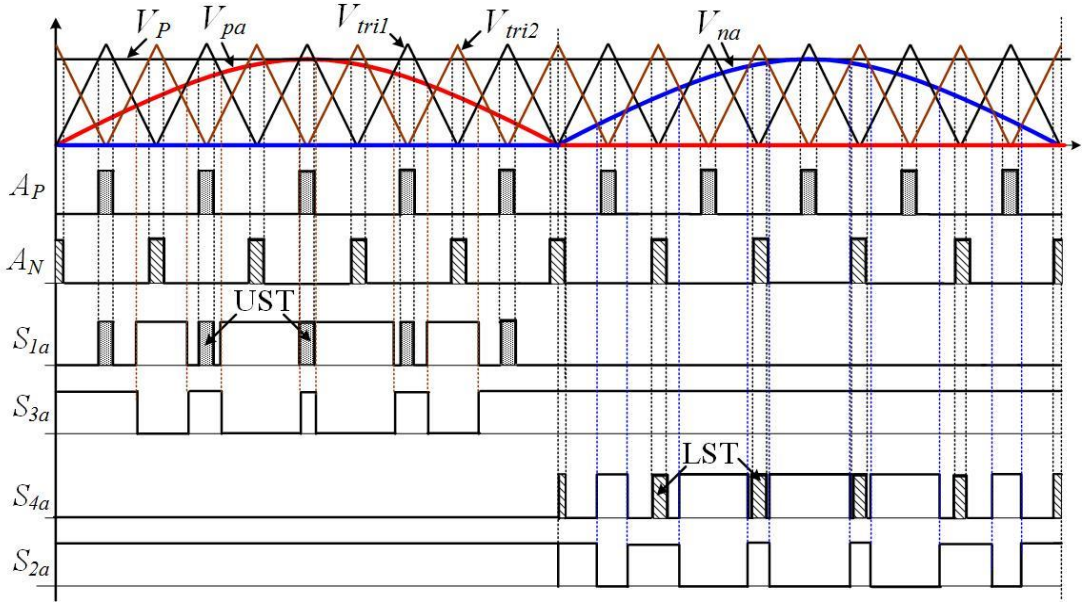


Fig. 14. Switching patterns of modulation technique.

Fig. 14 depicts the modified modulation technique based on an alternative phase opposition disposition (APOD) [35] for a-phase of the two proposed topologies to generate a boosted ac output voltage. As shown in Fig. 14, there are two carrier signals V_{tri1} and V_{tri2} with a 180° phase shift and the shoot-through envelope signal V_P. From three-phase sinusoidal reference signals, V_{ref_x} (x = a, b, or c), the three-phase positive and negative modulation signals V_{px} and V_{nx} (x = a, b, or c) can be obtained as

$$V_{px} = \frac{1}{2}(|V_{ref\_x}| + V_{ref\_x}) \tag{36}$$

$$V_{nx} = \frac{1}{2}(|V_{ref\_x}| - V_{ref\_x}) . \tag{37}$$

The pairs S_{1x}/S_{3x}, which are switched complementary, are generated by comparing the signal V_{px} with a carrier signal V_{tri1}. When the signal V_{px} is lower than V_{tri1}, the switch $S_{3x}$is turned on and the switch S_{1x} is turned off. The pairs S_{2x}/S_{4x}, which are switched in a complementary way, are generated by comparing the signal V_{nx} with a carrier signal V_{tri2}. When the signal V_{nx} is lower than V_{tri2}, the switch S_{2x} is turned on and the switch S_{4x} is turned off. The UST and LST signals can be produced by comparing the signal V_P with V_{tri1} and V_{tri2}, respectively. The UST state is inserted into the PWM signal of S_1 ain the positive reference signal period, and the LST state is inserted into the PWM signal of S_4 ain the negative reference signal period, in order to achieve a neutral-point voltage balance by balancing two series capacitor voltages.

4.2 Circuit block diagram for PWM generation for proposed topologies

Fig. 15 shows a logic circuit for generating 12 PWM signals from the three-phase reference signal V_{ref_x} and the shoot-through envelope signal V_P. The signals S_{px} and S_{nx} (x = *a*, *b*, or *c*) are utilized to insert the UST or LST state according to the polarity of the reference signal of each phase. The proposed modulation technique for the proposed topologies can be easily implemented by a simple logic circuit.

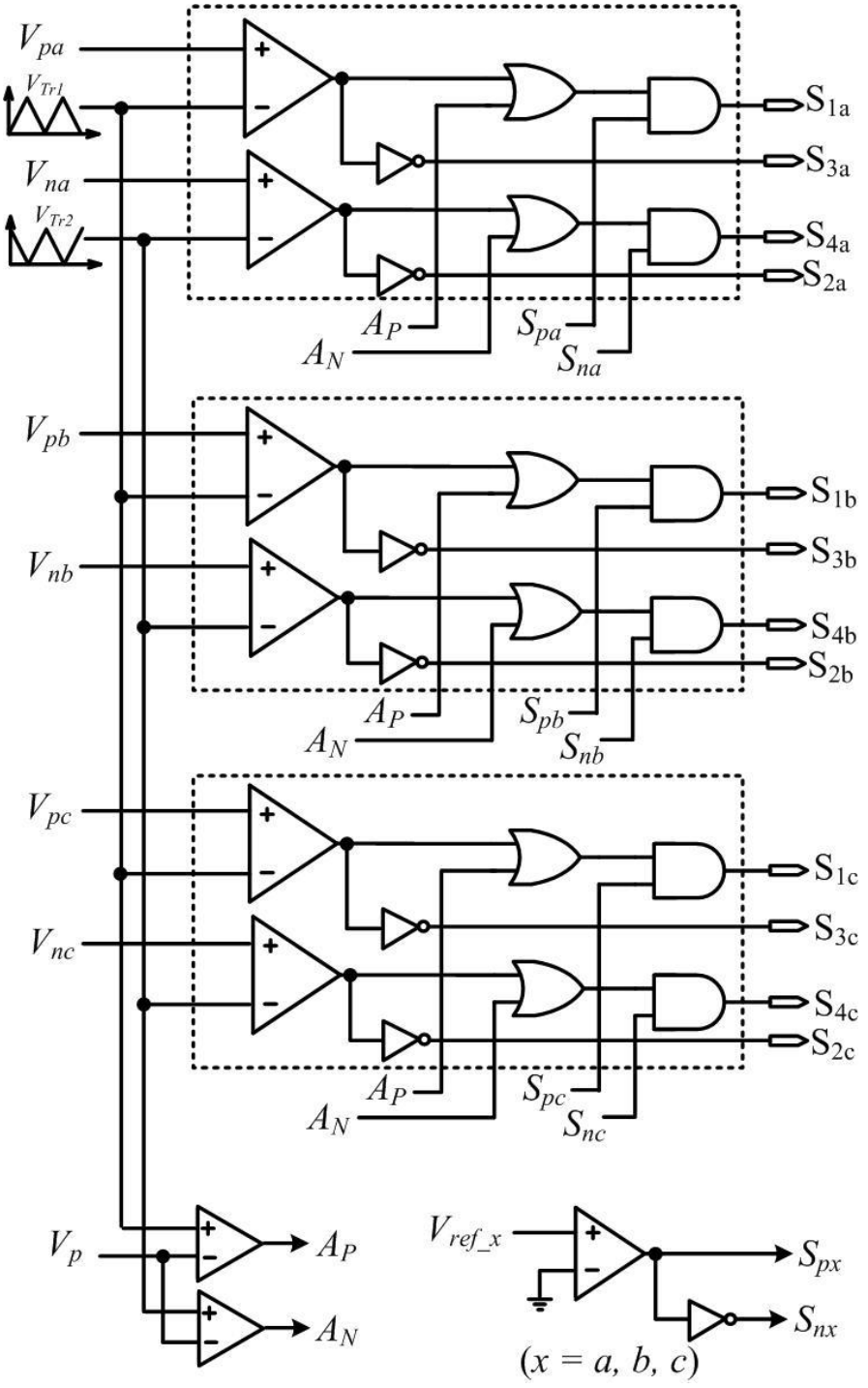


Fig.15. Circuit block diagram for PWM generation.

CHAPTER 5

SIMULATION RESULTS

The performances of the two proposed topologies are demonstrated with simulation and experimental results. One or two dc sources of 40V are embedded and the switching frequency of the 3LTI is 5 kHz. The list of the circuit parameters used for the simulation and experimental verification of the proposed topologies is given as follows:

- MZS network: $C_1 = C_2 = 1000$ µF, $C_3 = C_4 = 500$ µF, $L_1 = L_2 = 1$mH.
- Three-phase LC filter: $L_f = 0.6$ mH, $C_f = 50$ µF.
- Three-phase RL load: $R = 50\ \Omega$, $L = 1.2$ mH.

5.1 PSIM program for simulation circuits

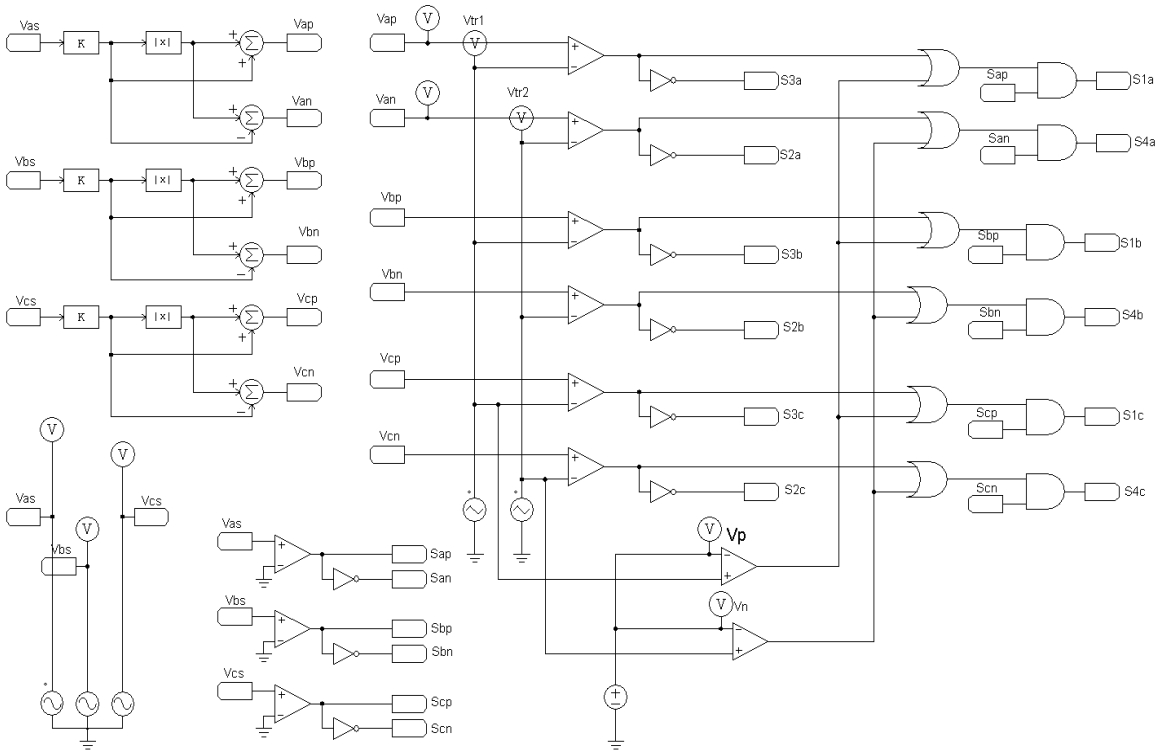
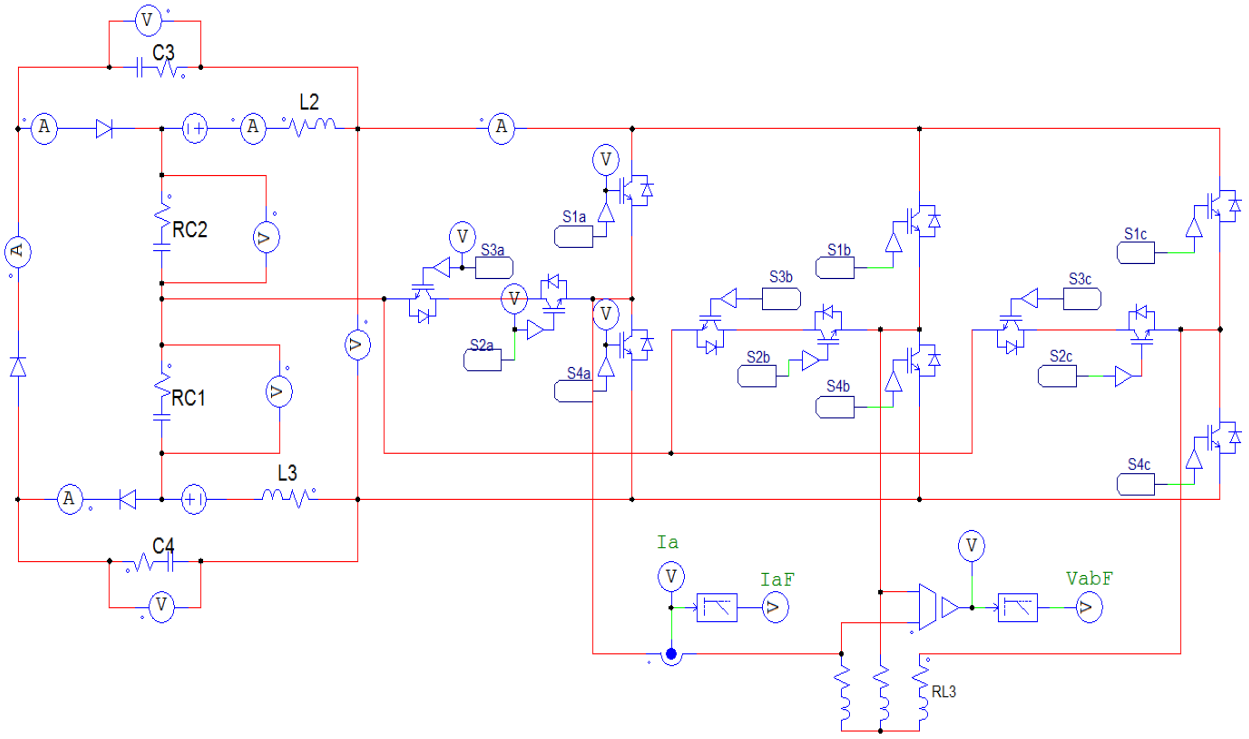
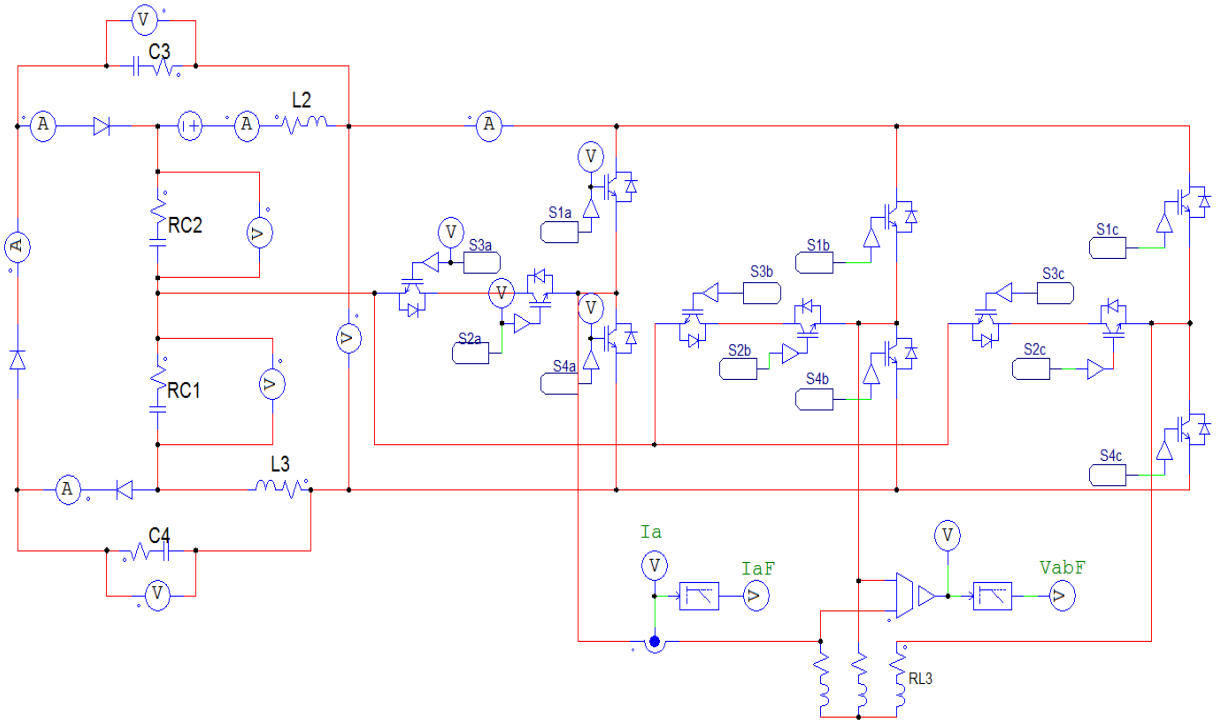


Fig. 16. PSIM program for gating signal generation circuit.



(a) SEMZS-3LTI



(b) AEMZS-3LTI

Fig. 17. PSIM program of power circuits of both topologies.

The simulations are carried out by using the PSIM program. Fig. 16 shows the PWM gating signal generation circuit in the PSIM program implemented from the logic circuit shown in Fig. 14. Fig. 17 shows the PSM program of the power circuits of two proposed topologies, using the same modified modulation technique shown in Fig. 16.

5.2 Simulation results

5.2.1 Simulation results of the SEMZS-3LTI

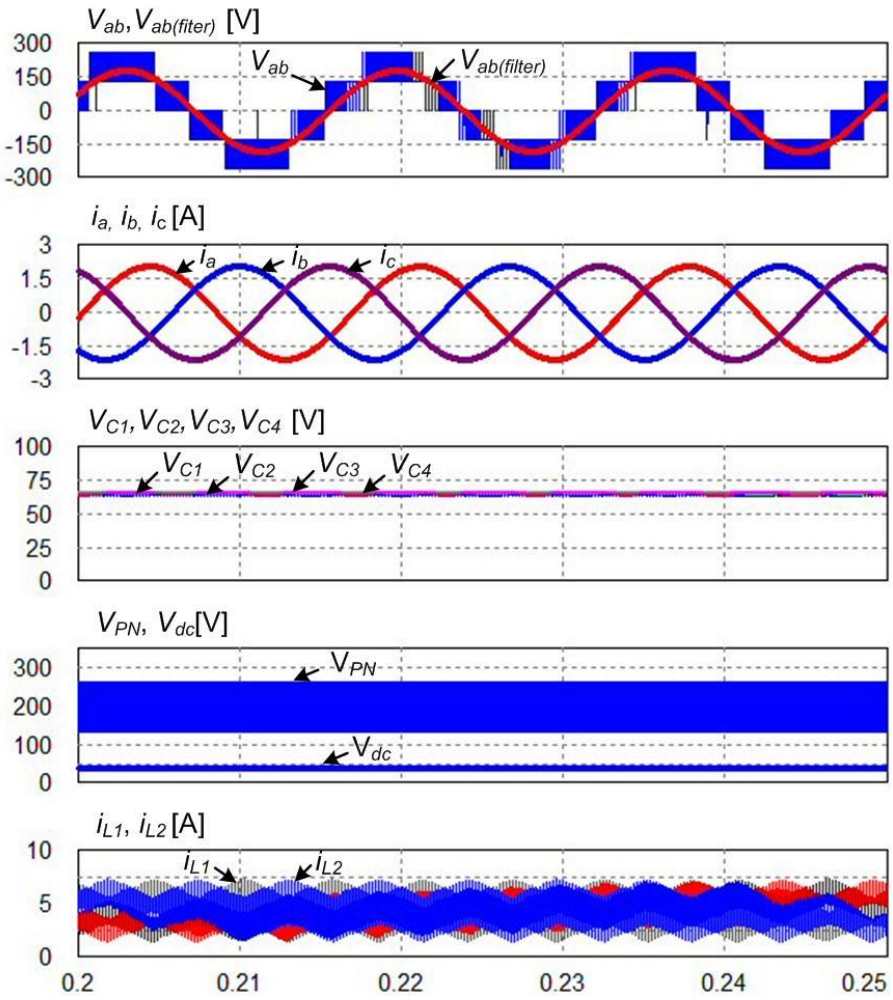


Fig. 18. Simulation results of SEMZS-3LTI when M = 0.8 and D = 0.2.

Fig. 18 shows the simulation results of the proposed SEMZS-3LTI topology when the modulation index M = 0.8 and D = 0.2. As shown in Fig. 18, the unfiltered ac output line-to-line voltage has five voltage steps, and the ac output voltage filtered by the LC filter of 128 V_{rms} is generated. Four capacitors have nearly the same average voltage of 65 V. The dc-link voltage is boosted to 260 V from the two dc sources of 40 V. Two inductor currents i_{L1} and i_{L2}, which are identical with two dc input currents, are continuous.

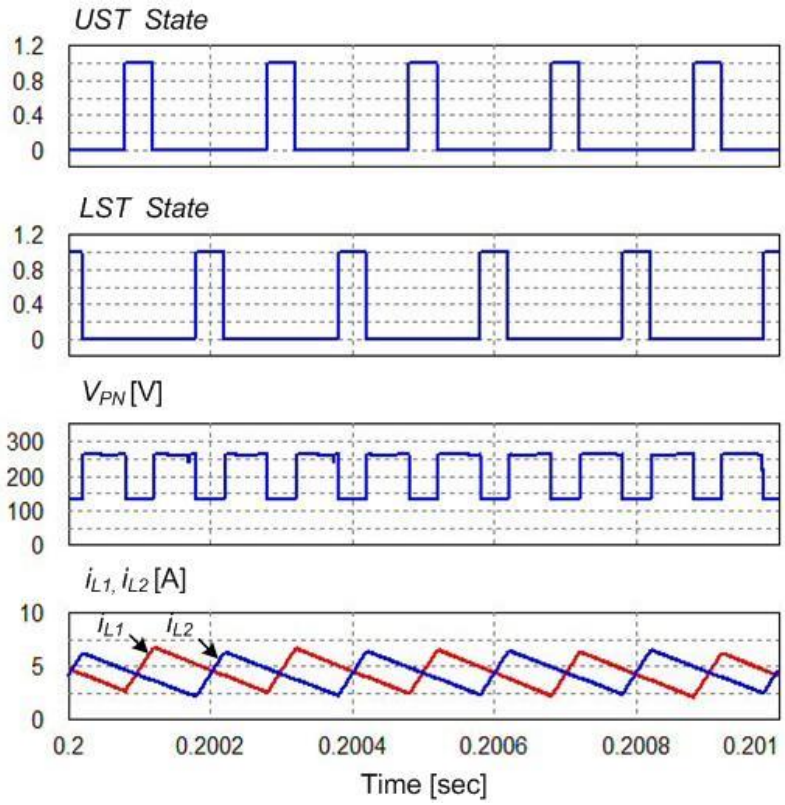


Fig. 19. Simulation results of SEMZS-3LTI when M = 0.8 and D = 0.2.

Fig. 19 shows the simulation results for two shoot-through states, dc-link voltage, and the inductor currents. From Fig. 19, the inductor currents i_{L1} and i_{L2} increase during UST and LST state, respectively, thus charging energy for each inductor. Two inductor currents decrease during NST state. The dc-link voltage during two shoot-through states is half of the peak dc-link voltage.

5.2.2 Simulation results of the AEMZS-3LTI

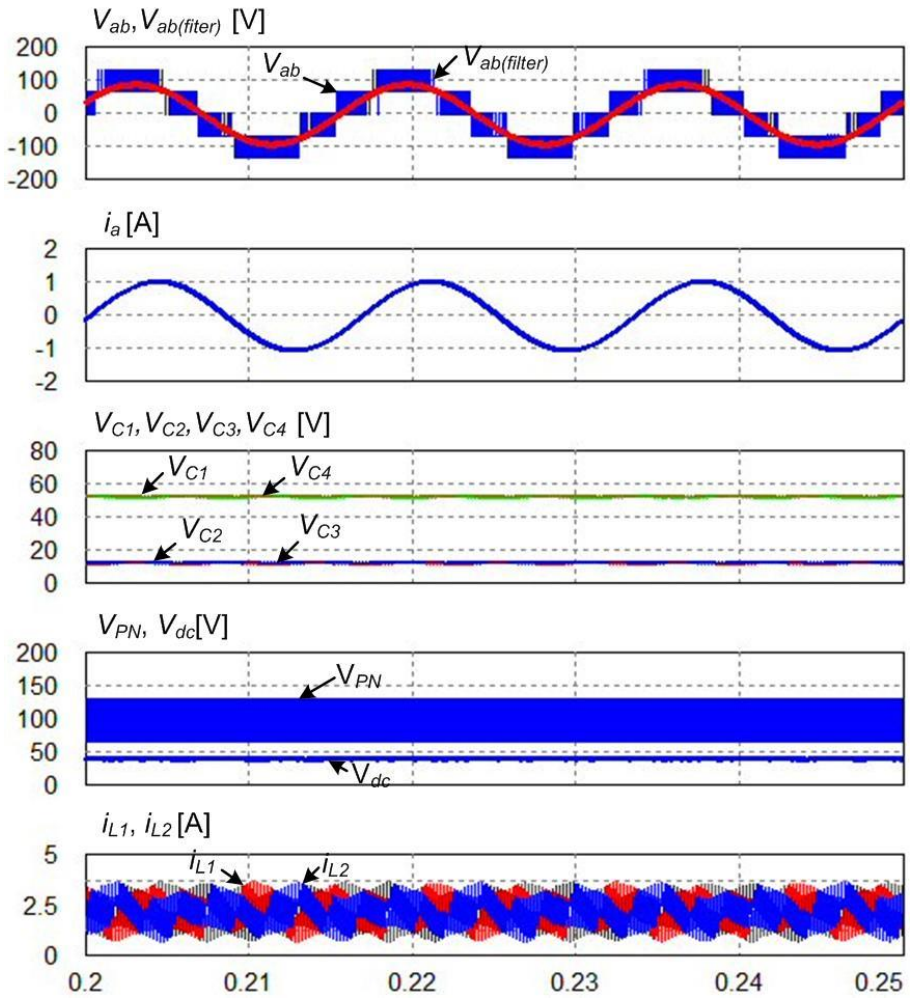


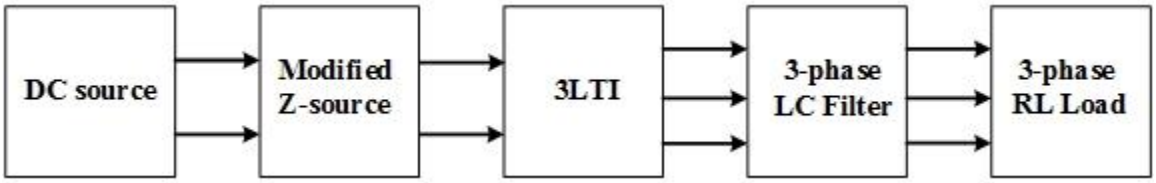
Fig. 20. Simulation results of AEMZS-3LTI when M = 0.8 and D = 0.2.

Fig. 20 shows the simulation results of the proposed AEMZS-3LTI topology when M = 0.8 and D = 0.2, which are the same parameters used for the simulation results of the SEMZS-3LTI topology. The rms value of the filtered ac output voltage and the peak dc-link voltage are 64 V and 130 V, respectively, which are half of those of the SEMZS-3LTI topology. The average value of the two capacitor voltages C_1 and C_4 is 52 V. The average voltage of C_2 and C_3 is 12 V, which is the value of dc input voltage (40 V) lower than the average voltage of C_1 and C_4.

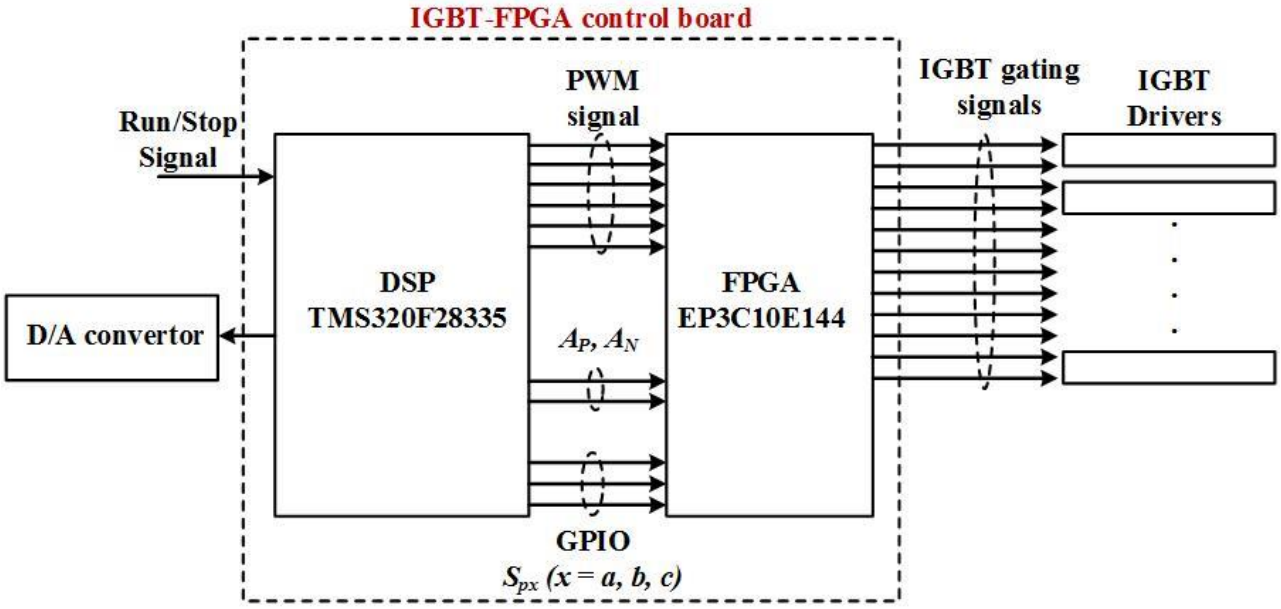
CHAPTER 6

EXPERIMENTAL RESULTS

6.1 Hardware configuration



(a) Structure of power circuit



(b) Structure of DSP-FPGA control board

Fig. 21. Hardware configuration.

Fig. 21(a) illustrates the structure of power circuits of both topologies. The power circuits consist of dc sources, modified-Z-source impedance network, 3LTI, 3-phase LC filter, and 3-

phase RL load. The AEMZS-3LTI embeds a single dc source whereas the SEMZS-3LTI embeds two dc sources. The power circuits are controlled by the DSP-FPGA control board.

Fig. 21(b) shows the connection between the DSP and the FPGA in the control board. The DSP generates six PWM signals, the UST and LST states A_P and A_N, and signals of the polarity of the reference voltage S_{px} and S_{nx} (x = a, b, or c). The DSP transmits six PWM signals and two shoot-through state signals A_P and A_N to FPGA through EPWM pins and it transmits three positive reference voltage signals S_{px} (x = a, b, or c) to FPGA through the general-purpose I/O port. The FPGA generates 12 gating signals including the UST and LST states by using the signals received from the DSP. The insulated gate bipolar transistor (IGBT) gating signals are transmitted to the IGBT driver circuits via the fiber optics.

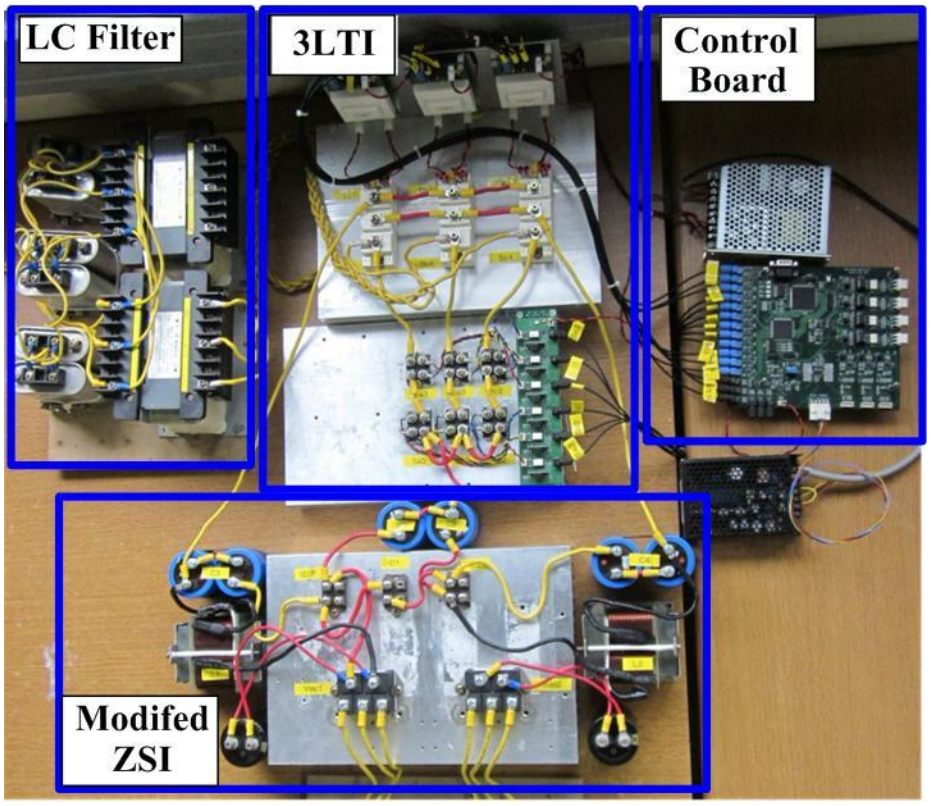
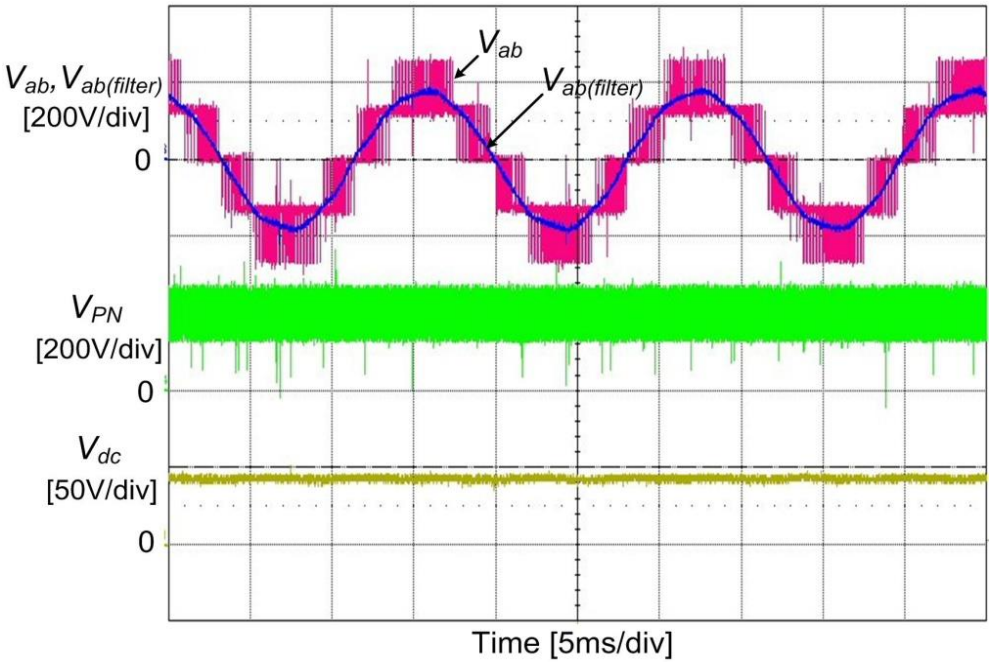


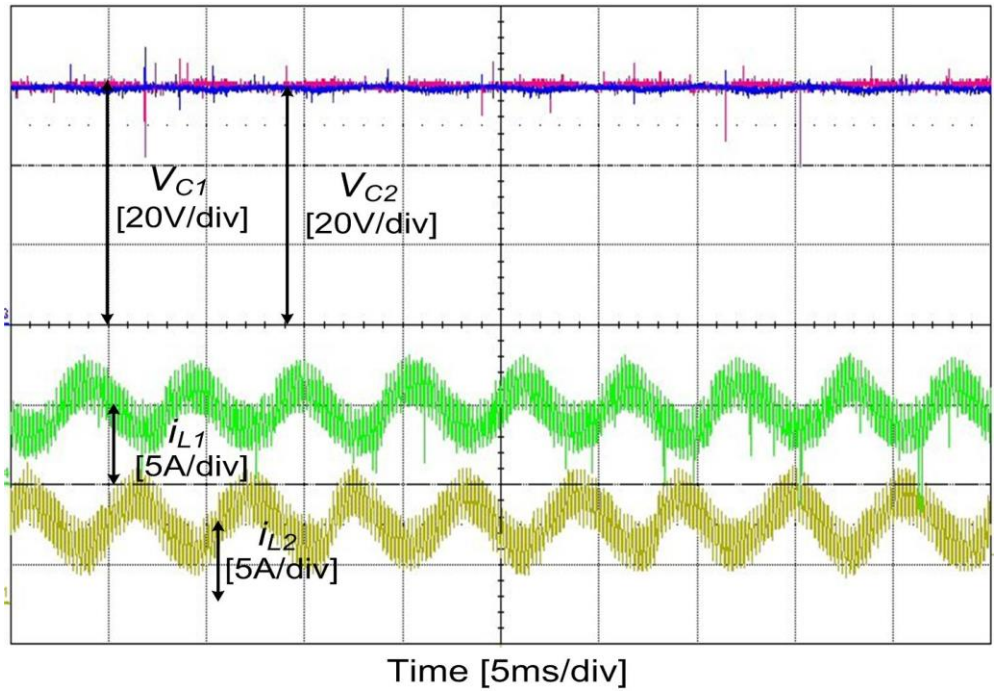
Fig. 22. Photograph of the experimental setup.

Fig.22 depicts an experimental prototype built-in laboratory to further verify the performances of proposed topologies. The prototype consists of a control board implemented by 32-bit DSP TMS320F28335 and FPGA, 3LTI with 12 IGBTs, a modified Z-source impedance network, a three-phase LC filter, and a resistive-inductive load. Two dc voltage sources are built by using a separate ac voltage source and diode rectifier. The difference in the structure of two topologies is that the AEMZS-3LTI circuit includes one dc input and SEMZS-3LTI includes two dc input.

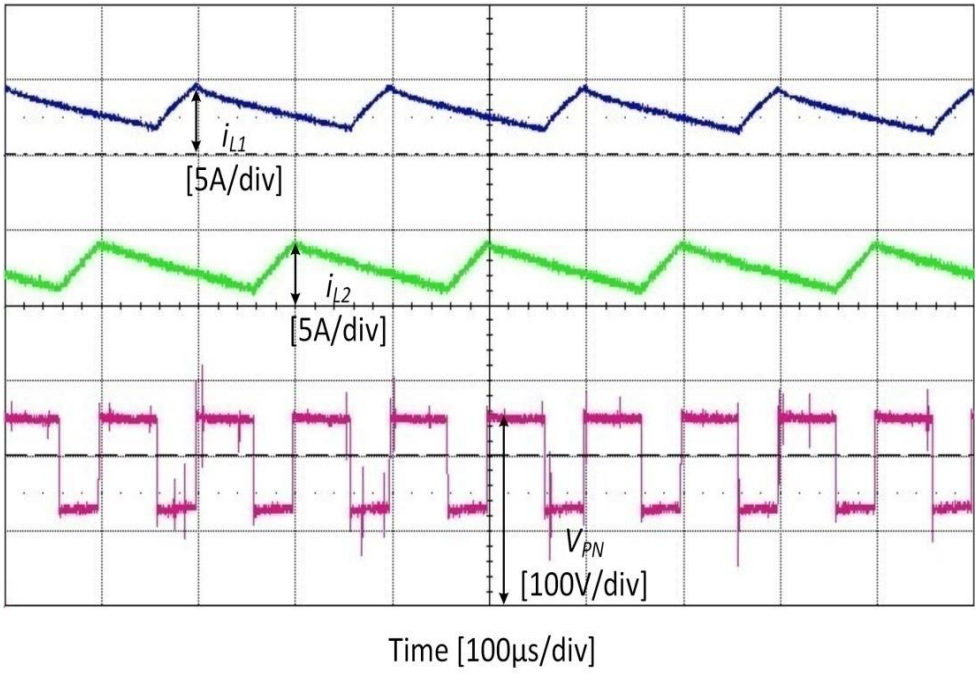
6.2 Experimental results of two proposed topologies



(a) Ac output voltages, dc-link voltage and dc input voltage



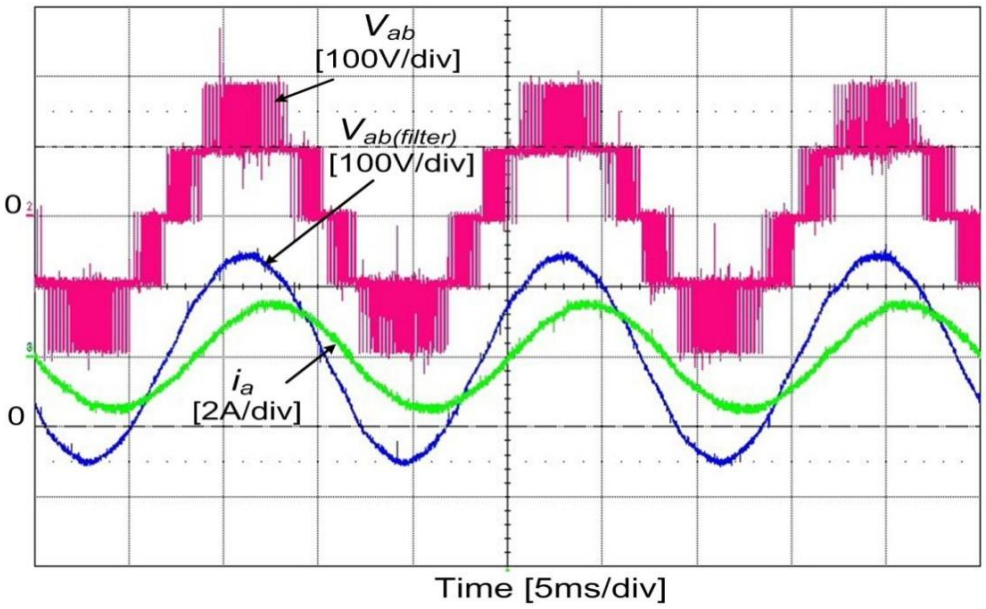
(b) Two capacitor voltages and inductor currents



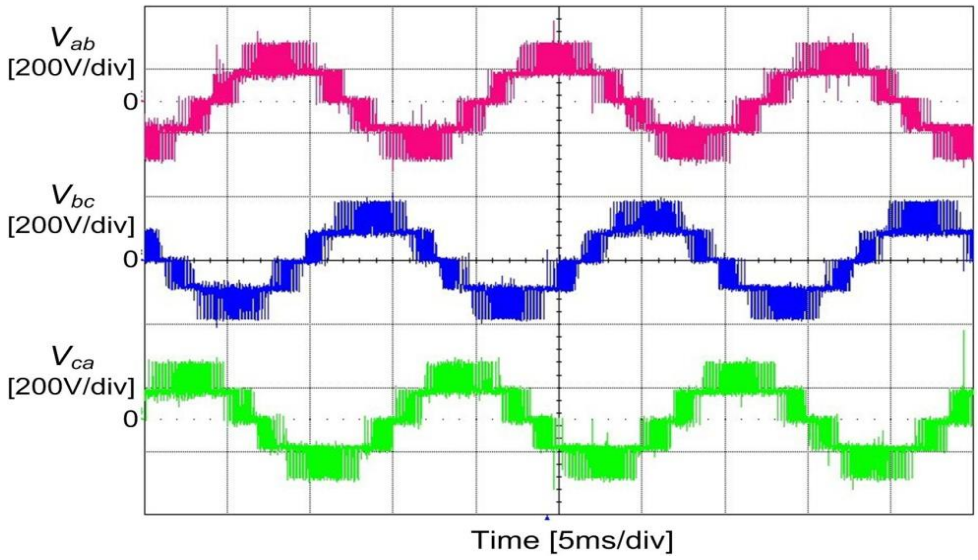
(c) Two inductor currents and dc-link voltage

Fig.23. Experimental results of SEMZS-3LTI when M = 0.8 and D = 0.2.

Fig. 23 shows the experimental results of the SEMZS-3LTI topology at the same operating conditions as the simulation results shown in Fig. 18. From Fig. 23(a), the generated line-to-line ac output voltage is 124 V_{rms} and the dc-link voltage is boosted to 250 V, which is 6.25 times the dc input voltage of 40 V. From Fig. 23(b), the voltage of two series capacitors is balanced with 62 V and two dc source currents are continuous. The inductor currents i_{L1} and i_{L2} increase during UST and LST states and they decrease during NST state as shown in Fig. 23(c).



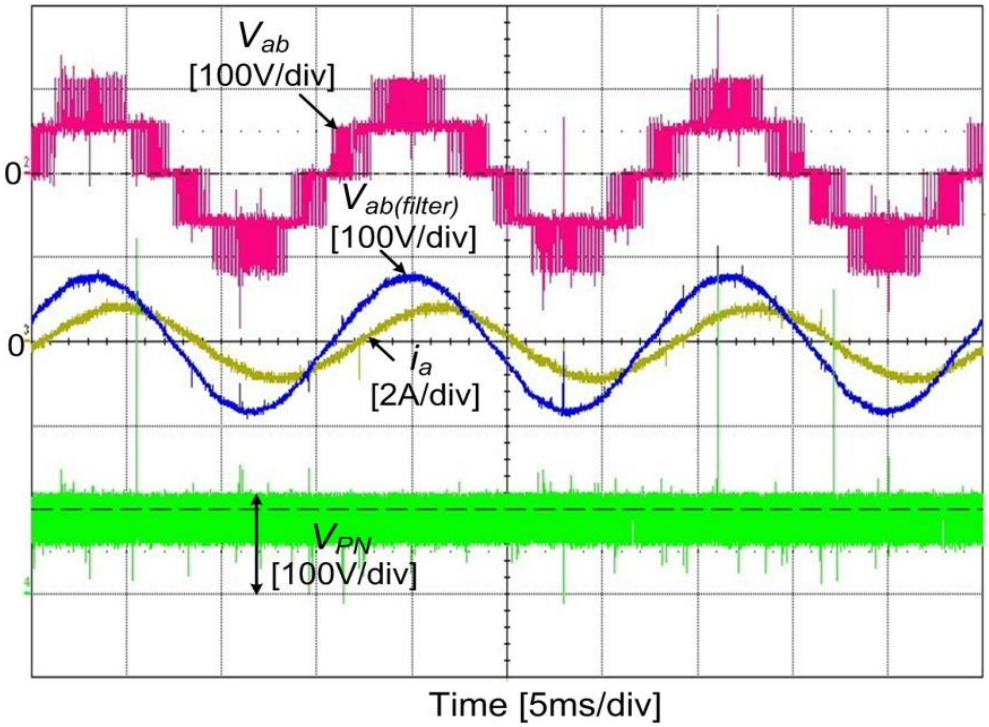
(a) Ac output voltage and current



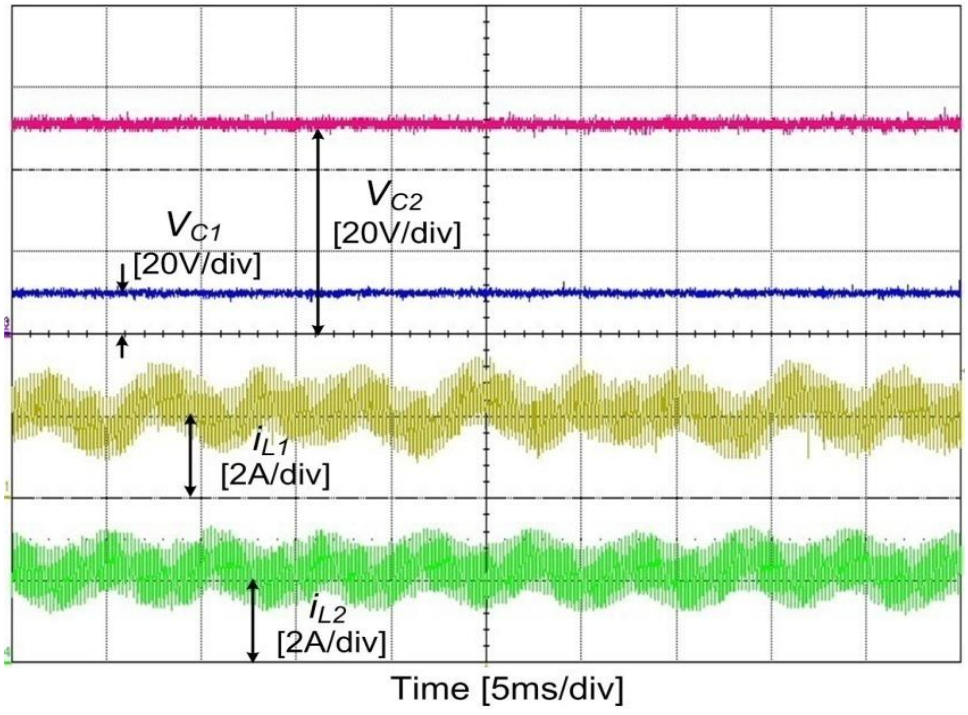
(b) Three-phase ac output voltages

Fig.24. Experimental results of SEMZS-3LTI when M = 0.9 and D = 0.1.

Fig. 24 shows the experimental results of the SEMZS-3LTI topology when M increases from 0.8 to 0.9 and D decreases from 0.2 to 0.1. In Fig. 24(a), in spite of the increase of M, the decrease of D by 0.1 results in reducing the ac output voltage to $105V_{rms}$. The balanced three-phase ac output voltages are shown in Fig. 24(b).



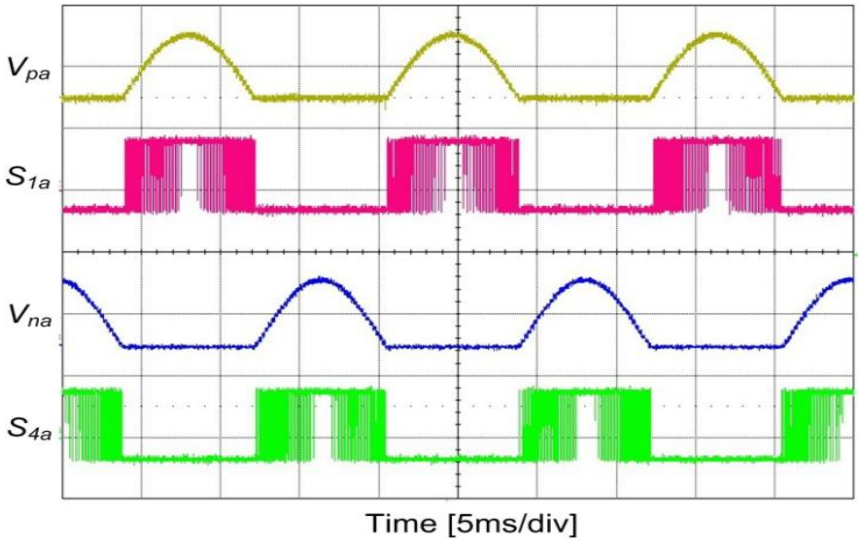
(a) Ac output voltage and current and dc-link voltage



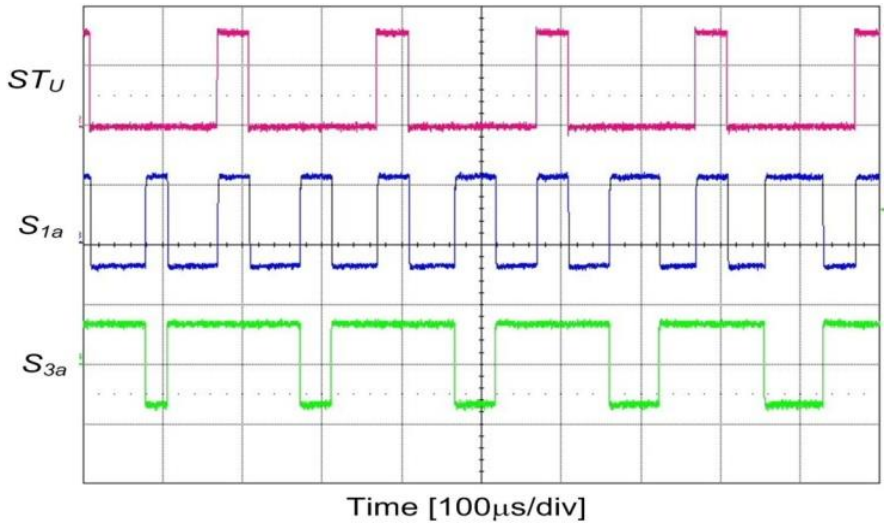
(b) Two capacitor voltages and inductor currents

Fig.25. Experimental results of AEMZS-3LTI when M = 0.8 and D = 0.2.

Fig. 25 shows the experimental results of the AEMZS-3LTI topology when M = 0.8 and D = 0.2. Both the ac output voltage and dc-link voltage are only half of those of the SEMZS-3LTI topology under the same M and D shown in Fig. 23. The average values of V_{C1} and V_{C2} are 10V and 50V, respectively. The voltage difference between two capacitors C_1 and C_2 is identical with the value of the dc input voltage embedded at the upper shell of the MZS network.



(a) Positive and negative modulation signals and gating signals S_{1a} and S_{4a}



(b) UST state and gating signals S_{1a} and S_{3a}

Fig.26. A-phase gating signals.

Fig. 26 describes the a-phase gating signals with the modulation signals and UST state. Fig. 26(a) shows the positive and negative modulation signals and gating signals S_{1a} and S_{4a}. The switches S_{1a} or S_{4a} have only modulated their pulse width when a reference signal is either positive or negative, respectively. From 26(b), the pairs S_{1x}/S_{3x} are switched complementary and the UST state is only inserted at the signal S_{1a}.

CHAPTER 7
CONCLUSION

This paper proposed two types of topologies known as AEMZS-3LTI and SEMZS-3LTI. They are designed by integrating a modified-Z-source impedance network to the traditional 3LTI, and embedding either one or two dc sources in the impedance network. The proposed topologies provide a highly boosted ac output voltage with three voltage levels and ensure a continuous dc source current by embedding the dc source(s) without the need for any extra filter. Compared to other topologies combining the impedance network and 3LTI, the SEMZS-3LTI topology has a boost factor by twice or four times higher and the lowest ratio of voltage stress across capacitors to the ac output voltage. The upper and lower shoot-through states are effectively adjusted and two series capacitor voltages are balanced by using a modified modulation technique implemented by a simple logic circuit. An experimental prototype has been built to well validate the performances of the two proposed topologies and modulation techniques. The proposed topologies are able to apply to the renewable generation systems with low voltage renewable energy sources such as the fuel-cells or the photovoltaic arrays.

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[ABSTRACTS]

Three-phase Embedded Modified-Z-Source Three-Level T-Type Inverters

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Two topologies are designed by combining a modified Z-source impedance (MZS) network consisting of three diodes, two inductors and four capacitors to the traditional three-level T-type inverter (3LTI), and embedding either one or two dc sources in the impedance network, which are named as asymmetrical embedded MZS-3LTI (AEMZS-3LTI) and symmetrical embedded MZS-3LTI (SEMZS-3LTI). The proposed topologies provide a highly boosted ac output voltage with five voltage levels and ensure a continuous dc source current by adopting the embedded concept. In comparison to other topologies combining the impedance network and 3LTI, the proposed SEMZS-3LTI topology has two times higher boost factor and the lowest ratio of voltage stress across capacitors to the ac output voltage. The modulation technique is proposed for effectively controlling the upper and lower shoot-through states with a simple logic circuit and balancing two series capacitor voltages. The validity of the proposed topologies and the modulation technique is demonstrated through simulation and experimental results.